Very Small Satellite Design for Space Sensor Networks

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Summary

An investigation of very small satellite miniaturisation techniques is presented, focusing on enabling sub-kilogram technologies targeted at space sensor network applications. Distributed space mission concepts are emerging for scientific and remote sensing applications requiring massively distributed systems, analogous to proliferating terrestrial wireless sensor networks. This particular architecture will enable observation of real-time multi-point phenomena.

Space economics and environmental concerns dictate a cost-effective mass-producible low-mass satellite for brief but essential missions in low Earth orbit. Existing and emerging very small satellite technologies have been investigated, assessed, and compared, where power generation and payload volume are the key performance metrics. Two novel design methodologies have been developed, simulated, and verified through functional and environmental testing of hardware.

SpaceChip, inspired by the satellite-on-a-chip vision, is a monolithic heterogeneous system-on-a-chip integration approach. SpaceChip proves widely applicable to sensor networks in hostile environments, including space, which require simple sensors and sub-kilometre separations. Five SiGe BiCMOS prototype chips have been fabricated which show promising results for two previously undeveloped subsystems. A method has been investigated for on-chip series connection of solar cells yielding a 3.4% efficient system-on-a-chip power supply. Furthermore, an environmentally-tolerant microprocessor design technique was developed that verifies the synergy of radiation hardening by design and asynchronous logic.

PCBSat is proposed as a satellite-on-a-PCB miniaturisation approach focused on deriving the smallest practical satellite within the context of space sensor networks and constrained to the use of commercial components, processes, and deployment systems. The concept has been validated by flight model development and test, measuring 10×10×2.5 cm and 300 grams, for $10,000 to orbit in quantity. PCBSat emerges as an optimal tradeoff between cost and performance.

A case study investigation of ionospheric plasma depletions, known to cause problematic navigation and communication outages, provided a comparison vehicle of all technologies considered in this effort. A demonstration mission based on PCBSat has been selected by NASA for launch in 2010. This research has advanced the state-of-the-art by providing new demonstrated cost-effective miniaturisation approaches enabling sensor network architectures.

Key words: distributed satellite system, distributed space mission, wireless sensor network, satellite miniaturisation, fractionation, picosatellite, satellite-on-a-chip, SiGe BiCMOS solar cell

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The views expressed in this document are those of the author and do not reflect the official policy or position of the United State Air Force, Department of Defense, or the U.S. Government.

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List of Abbreviations

ADC	Analogue-to-Digital Converter
ADCS	Attitude Determination and Control
AFSM	Asynchronous Finite State Machine
AIAA	American Institute of Aeronautics and Astronautics
AIT	Assembly, Integration, and Test
AM0	ASTM E-490 Zero Air Mass Solar Spectral Irradiance (1366.1 W/m^2)
AMSAT	Amateur Satellite
AOCS	Attitude and Orbit Control Subsystem
AMS	austriamicrosystems
ASIC	Application Specific Integrated Circuit
ASTM	American Society for Testing and Materials
BC	Ballistic Coefficient
BCR	Battery Charge Regulator
BJT	Bipolar Junction Transistor
C/NOFS	Communication and Navigation Outage Forecasting System
CAD	Computer Aided Design
CCD	Charge Coupled Device
CG	Centre of Gravity
CMOS	Complementary Metal-on-silicon
Comm	Communications Subsystem
COSA	Co-Orbiting Satellite Assistant
COTS	Commercial off the Shelf
CP	Centre of Pressure
CTS	Clock Tree Synthesis
CPU	Central Processing Unit

DAC	Digital-to-Analogue Converter
DARPA	Defense Advanced Research Projects Agency
DH	Data Handling Subsystem
DMC	Disaster Monitoring Constellation
DMSP	Defense Meteorological Satellite Program
DS	Double Star
EMI	Electromagnetic Interference
EMP	Electromagnetic Pulse
EOS	Earth Observation System
EPS	Electrical Power Subsystem
ESA	European Space Agency
EU	European Union
FPGA	Field Programmable Gate Array
GaAs	Gallium Arsenide
GCR	Galactic Cosmic Rays
GEO	Geostationary Orbit
GPS	Global Positioning System
GSE	Ground Support Equipment
GSM	Global System for Mobile Communication
HDL	Hardware Description Language
IC	Integrated Circuit
I/O	Input/Output
IR	Infrared
ISM	Instrumentation, Scientific, and Medical
ISP	In System Programming
ISS	International Space Station
LEO	Low Earth Orbit
MAX	Maxim Integrated Products, Inc.

MCM	Multi-chip Module
MEMS	Microelectromechanical Systems
MEO	Medium Earth Orbit
MESA	Miniaturized ElectroStatic Analyzer
NASA	National Aeronautics and Space Administration
nMOS	n-type Metal on Silicon
NPN	n-p-n Silicon Junction
NRE	Non-Recurring Engineering
OOK	On-Off Keying
op amp	Operational Amplifier
OPAL	Orbiting Picosatellite Activated Launcher
P-POD	Poly Picosatellite Orbital Deployer
PCB	Printed Circuit Board
PCBSat	Satellite-on-a-PCB Design Methodology
pMOS	p-type Metal on Silicon
PPT	Peak Power Tracker
PWM	Pulse Width Modulated
RBF	Remove Before Flight
RF	Radio Frequency
RFID	Radio Frequency Identification
RHBD	Radiation Hardening by Design
RISC	Reduced Instruction Set Computer
RX	Receiver
S35	SiGe BiCMOS 0.35 μm Process
SCR	Silicon Controlled Rectifier
SEE	Single Event Effects
SEL	Single Event Latchup
SET	Single Event Transient

SEU	Single Event Upset
Si	Silicon
SiGe	Silicon Germanium
SiP	System in Package
SMAD	Space Mission Analysis and Design
SoC	System-on-a-Chip (SoC)
SOI	Silicon on Insulator
SpaceChip	Satellite-on-a-Chip Design Methodology
SPI	Serial Peripheral Interface
SSC	Surrey Space Centre
SSPL	Space Shuttle Picosatellite Launcher
SSTL	Surrey Satellite Technology, Ltd.
STK	Satellite Tool Kit
TCS	Thermal Control Subsystem
TID	Total Ionizing Dose
TLM	Telemetry
TMR	Triple Modular Redundancy
TRL	Technology Readiness Level
TX	Transmit
UHF	Ultra High Frequency
UMB	Umbilical
USART	Universal Synchronous-Asynchronous Receiver/Transmitter
UV	Ultraviolet
VHF	Very High Frequency
WINS	Wireless Integrated Network Sensors
WSI	Wafer Scale Integration

List of Symbols

a	=	semi-major axis, m or acceleration, $m \cdot s^{-2}$
alb	=	albedo, 0.30 ± 0.05
α	=	absorptivity
A	=	surface area, m^2
A_{sa}	=	required solar array area, m^2
BC	=	ballistic coefficient
C	=	capacitance, F
C_d	=	drag coefficient
C_r	=	battery capacity required, A·hr
c	=	speed of light, 3×10^8 $m \cdot s^{-1}$
DOD	=	depth of discharge
ε	=	emissivity
f	=	frequency, Hz
F	=	force, N
F_d	=	drag force, N
F_{srp}	=	solar radiation pressure force, N
F_p	=	flat plate view factor
G_r	=	receiver gain
G_s	=	solar flux, 1418 $W \cdot m^{-2}$ to 1326 $W \cdot m^{-2}$
G_t	=	transmitter gain
h	=	altitude, km
I_d	=	inherent degradation
k	=	Boltzmann's constant, 1.381×10^{-23} $J \cdot K^{-1}$
K_a	=	spherical view factor
L_s	=	free space loss

λ	=	wavelength, m
$\mu_{\oplus}$	=	Earth gravitational parameter, 3.986×10^{5} km^{3}·s^{-2}
m	=	mass, kg
n	=	transmission efficiency between battery and load
η	=	solar cell efficiency
P	=	period, s
P_{BOL}	=	beginning of life solar array power output, W·m^{-2}
P_e	=	power required in eclipse, W
P_s	=	power required in sun, W
P_{sa}	=	power required from solar array, W
P_t	=	transmitter power, W
q_I	=	Earth infrared flux, 237 ± 21 W·m^{-2}
r	=	reflection factor
R	=	data rate, bits per second
$R_{\oplus}$	=	Earth radius, 6,378,136 m
ρ	=	angular radius, deg or atmospheric density, kg·m^{-3}
S	=	range, m
σ	=	Stefan-Boltzmann's constant, 5.67×10^{-8} W·m^{-2}·K^{-4}
T_e	=	time in eclipse, s
θ	=	incidence angle, deg
T_s	=	time in sun, s
T_{sys}	=	system noise, dB·K
v	=	voltage, V or velocity, m·s^{-1}
w	=	energy, J
x	=	position, m
X_e	=	power transfer efficiency in eclipse
X_s	=	power transfer efficiency in sun

Chapter 1

1 Introduction

This thesis presents an investigation of very small satellite miniaturisation techniques, focusing on enabling sub-kilogram technologies targeted at space sensor network applications. The concept of satellite-on-a-chip is first investigated, which proves ideally suited for sensor networks in hostile environments with sub-kilometre separations, due to fundamental payload and power limitations. Satellite-on-a-printed circuit board is then investigated, based on commercial components, processes, and deployment systems, which ultimately demonstrates a viable cost-effective alternative that can support a range of meaningful unrealized space missions.

A *satellite* is defined as a natural or artificial object in motion around a more massive body, where this motion is defined as an *orbit*, enabled by the dominant force of gravity from the more massive body, as shown in Figure 1-1 [1]. The earliest depictions of artificial satellites date back to the 1800's and possibly before, but it was not until 1957 when this idea became reality through the launch of Sputnik 1. Mission requirements have grown considerably since then, which continually drive the mass and number of satellites upwards.

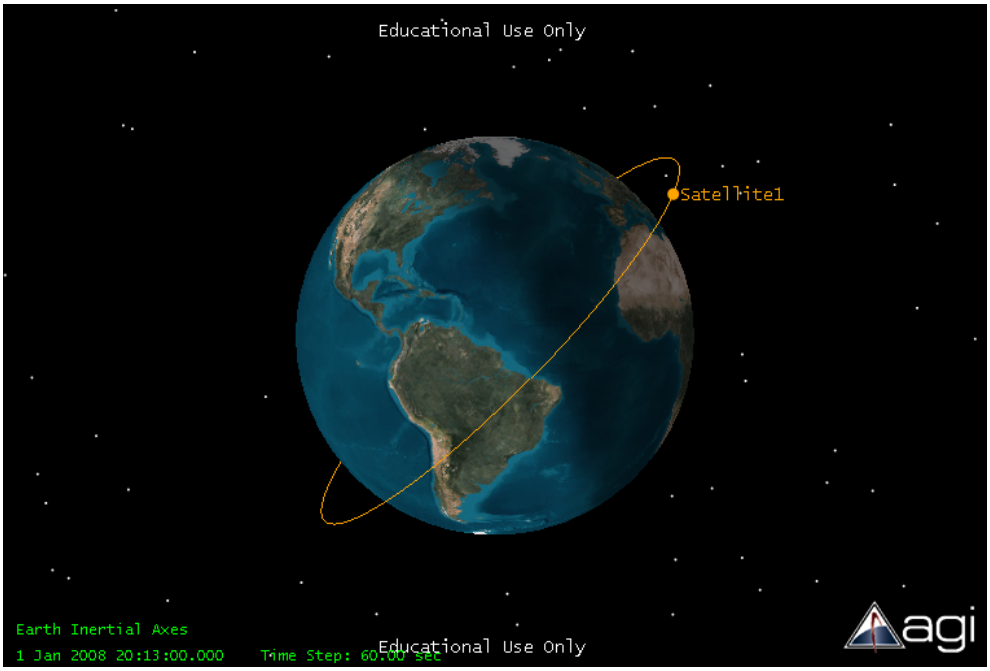

Figure 1-1. Notional Orbit

A system where two or more satellites function collectively to perform a task is defined as a distributed satellite system as illustrated in Figure 1-2. Perhaps the first *distributed space mission* was envisaged in 1945 [2], where a global communications system of three satellites was proposed, but it was not until 1963 when the first communications relay satellite was launched. There is a growing trend toward distributed missions where large numbers of satellites are required. For example, the largest active distributed mission currently on orbit employs a *constellation* of 66 satellites, providing global communication services to mobile users.

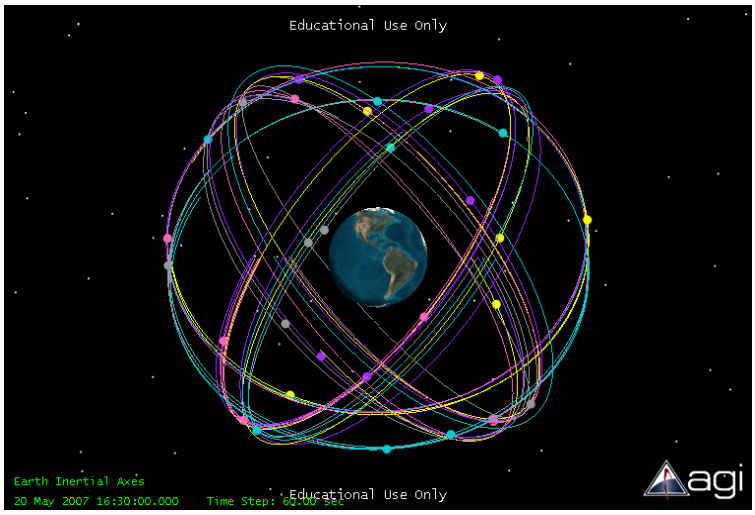

Figure 1-2. Notional Distributed Satellite System

Meanwhile, terrestrial *wireless sensor networks* are proliferating where numerous wireless sensor devices or *nodes* are distributed over large areas for a particular application, such as soil health monitoring and industrial process control [3]. Introduced as early as 1992, the phenomenal growth of terrestrial sensor networks suggests that space may be the next application domain. *Space sensor networks* could provide an unprecedented capability to investigate widespread phenomena.

Unlike terrestrial sensor nodes, satellites must survive the unique environment of space whilst undergoing complex orbital dynamics. The space environment is hazardous to spacecraft due to radiation, debris, and the thinning atmosphere. Additionally, space sensor networks require unusually large numbers of satellites, conceivably in the hundreds or thousands. However, most of the previously proposed missions lack practical hardware solutions.

Since the dawn of the space age in 1957, increasing mission requirements in this hostile environment have driven satellite mass from Sputnik's 84 kg to over 6,000 kg for some systems today. Consequently, cost and complexity have grown significantly, with some missions commanding multi-billion dollar budgets. Reversing this trend, a fast-growing small satellite industry, rooted in academia, has enabled increasingly capable and cost-effective space missions. Focusing on satellites with a mass below 500 kilograms, their success is based on embracing sensibly reduced requirements and leveraging commercial technologies.

The motivation of this research is to define the smallest practical satellite to enable space sensor networks by examining, developing, and comparing supporting technologies as illustrated in Figure 1-3. Economics dictate a low-mass, cost-effective, and mass-producible satellite, whilst politics dictate short-lived mission scenarios in low Earth orbit (LEO) to mitigate orbital debris. *This research proposes that leveraging innovative mass-production infrastructures of the vibrant personal electronics industry is the way forward to enable space sensor networks.*

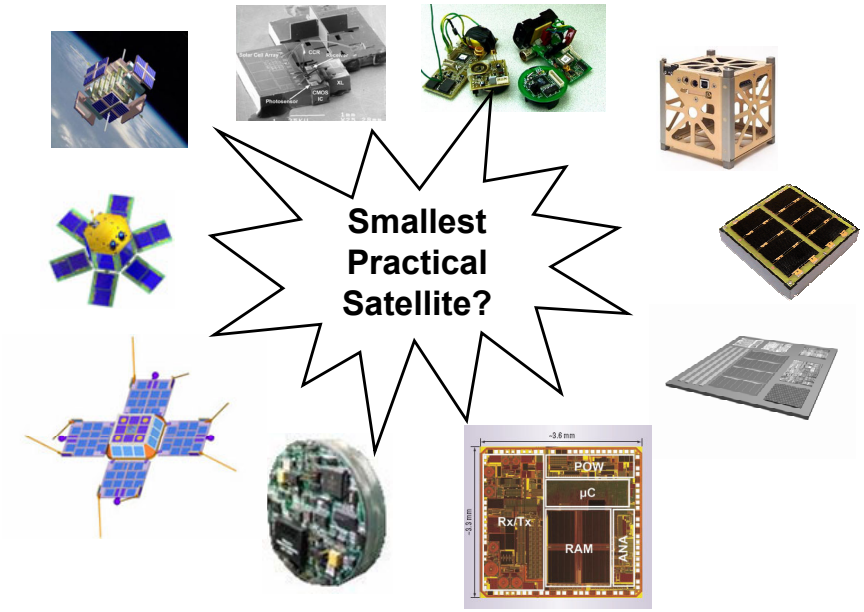

Figure 1-3. The Quest for the Smallest Practical Satellite

To the best of the author's knowledge, no one before has investigated in detail the mass-production of spacecraft using existing commercial infrastructures to enable a useful space sensor network concept. For example, several important space weather missions have yet to be realized due to the present inability to take simultaneous measurements of a phenomenon over a large volume. An example case study is considered, where a space sensor network could demystify ionospheric plasma depletions, which are thought to cause problematic navigation and communication signal *scintillation*, i.e. communication outages. Such a mission would greatly enhance commercial, government, and military sectors, which all depend on satellite communications and navigation for commerce, political stability, and military operations.

This type of scenario requires a constellation size at least an order of magnitude greater than existing distributed satellite systems, such as the Global Positioning System (GPS), which requires 24 satellites, and the IRIDIUM communications system, with 66 satellites. Considering that science missions typically have significantly smaller budgets, an unprecedented low-cost approach is required. Contemporary academic research in satellite miniaturisation is focused on developing complex and expensive manufacturing processes with maturing timelines of five to ten years to support distributed space missions with more demanding requirements.

1.1 Scope of Research

Emerging distributed communication and navigation missions appear to be moving toward more massive satellites to meet growing requirements and very profitable market demands. However, a range of proposed distributed remote sensing and scientific missions are found to be supportable by increasingly smaller satellites. *The scope of this research has been constrained to investigating very small satellites, which have a mass less than one kilogram, by targeting meaningful space sensor network missions with straightforward requirements and achievable goals.*

The range of existing very small satellite concepts are examined, beginning with standardised picosatellites, which are based on a traditional fabrication model. Microengineered aerospace systems focused on next-generation technologies and manufacturing processes, are then examined. Additionally, two previously undeveloped design approaches are revived. Firstly, the concept of *satellite-on-a-chip* (SpaceChip) is reassessed where two major building blocks are developed. Secondly, the concept of *satellite-on-a printed circuit board* (PCBSat), inspired by the earliest picosatellite attempts, is fully developed as a very small satellite miniaturisation approach. All concepts are compared using a case study mission to determine their practicality and cost-effectiveness.

1.2 Aims and Objectives

The overall aims of this research are:

- To advance the concept of space sensor networks
- To determine the smallest practical cost-effective satellite in this context

The objectives of this research supporting the overall aims are:

- Review and classify distributed space missions and systems
- Investigate existing and emerging very small satellite technologies
- Propose a meaningful space sensor network mission as a case study
- Determine the critical mission requirements and architecture for the case study mission
- Develop supporting satellite technologies and system concepts
- Validate the work by designing, building, and characterising very small satellite prototypes
- Compare existing and newly developed technologies in this research for mission suitability, cost effectiveness, and mass producibility

1.3 Research Novelty

This research contributes to the state of the art by:

- Identifying a range of sensor network missions that are enabled by very small satellites
- Conducting the first feasibility study of the satellite-on-a-chip concept
- Investigating a usable on-chip photovoltaic power supply for any system-on-a-chip
- Verifying an environmentally-tolerant design methodology for system-on-a-chip applications by combining radiation hardening by design and asynchronous logic
- Designing, building, characterising, and testing a very small satellite flight model prototype
- Comparing all very small satellite technologies for mission suitability and cost-effectiveness

1.4 Publications

The results of this research have been incrementally reported in the following publications:

1. D. J. Barnhart, T. Vladimirova, and M. N. Sweeting, "Very Small Satellite Design for Distributed Space Missions," *AIAA Journal of Spacecraft and Rockets*, vol. 44, no. 6, Nov.–Dec. 2007, pp. 1294–1306.
2. T. Vladimirova and D. J. Barnhart, "Towards Space Based Wireless Sensor Networks," in *Small Satellites: Past, Present, and Future*, H. Helvajian, Ed. Reston, VA: AIAA Press, 2008.
3. D. J. Barnhart, T. Vladimirova, and M. N. Sweeting, "Satellite-on-a-Chip: A Feasibility Study," in *Proc. Fifth Round Table on Micro/Nano Technologies for Space Workshop*, Nordwijk, The Netherlands, 2005, ESA WPP-255, pp. 728–735.
4. T. Vladimirova, X. Wu, K. Sidibeh, D. J. Barnhart, and A.-H. Jallad, "Enabling Technologies for Distributed Picosatellite Missions in LEO," in *Proc. First NASA/ESA Conf. on Adaptive Hardware and Systems*, Istanbul, 2006, pp. 330–337.
5. D. J. Barnhart, T. Vladimirova, and M. N. Sweeting, "Satellite-on-a-Chip Development for Future Distributed Space Missions," in *Proc. CANEUS Micro-Nano Technologies for Aerospace Applications Conf.*, Toulouse, France, 2006, Paper CANEUS 2006–11045.
6. D. J. Barnhart, T. Vladimirova, A. M. Baker, and M. N. Sweeting, "A Low-Cost Femtosatellite to Enable Distributed Space Missions," in *Proc. 57th Int. Astronautical Congress*, Valencia, Spain, 2006, Paper IAC–06–B5.6.06.

7. D. J. Barnhart, T. Vladimirova, and M. N. Sweeting, "System-on-a-Chip Design of Self-Powered Wireless Sensor Nodes for Hostile Environments," in *Proc. IEEE Aerospace Conf.*, Bozeman, MT, 2007, Paper 7.05.01.

8. T. Vladimirova, C. P. Bridges, G. Prassinos, X. Wu, K. Sidibeh, D. J. Barnhart, A.-H. Jallad, J. R. Paul, V. Lappas, A. Baker, K. Maynard, and R. Magness, "Characterising Wireless Sensor Motes for Space Applications," in *Proc. Second NASA/ESA Conf. on Adaptive Hardware and Systems*, Istanbul, 2007, pp. 43–50.

9. D. J. Barnhart, T. Vladimirova, M. N. Sweeting, R. L. Balthazor, L. C. Enloe, L. H. Krause, T. J. Lawrence, M. G. Mcharg, J. C. Lyke, J. J. White, and A. M. Baker, "Enabling Space Sensor Networks with PCBSat," in *Proc. USU/AIAA Small Satellite Conf.*, Logan, UT, 2007, Paper SSC07–IV–4.

10. W. W. Saylor, K. Smaagard, N. Nordby, and D. J. Barnhart, "New Scientific Capabilities Enabled by Autonomous Constellations of Smallsats," in *Proc. USU/AIAA Small Satellite Conf.*, Logan, UT, 2007, Paper SSC07–II–7.

11. D. J. Barnhart, T. Vladimirova, and M. N. Sweeting, "Design of Self-Powered Wireless System-on-a-Chip Sensor Nodes for Hostile Environments," in *Proc. IEEE Int. Symp. on Circuits and Systems*, Seattle, WA, 2008, pp. 824–827.

12. T. Vladimirova and D. J. Barnhart, "Heterogeneous System-on-a-Chip Design for Self-Powered Wireless Sensor Networks in Non-Benign Environments," Surrey Space Centre, University of Surrey, Guildford, United Kingdom, Rep. FA8655-06-1-3053, Mar. 2008.

13. D. J. Barnhart, T. Vladimirova, M. N. Sweeting, and K. S. Stevens, "Radiation Hardening by Design of Asynchronous Logic for Hostile Environments," *IEEE Journal of Solid-State Circuits*, submitted for publication.

14. D. J. Barnhart, T. Vladimirova, and M. N. Sweeting, "SiGe BiCMOS Photovoltaic Cells for System-on-a-Chip Power Supply Applications," *IEEE Electron Devices Letters*, submitted for publication.

15. D. J. Barnhart, T. Vladimirova, and M. N. Sweeting, "Very Small Satellite Design for Space Sensor Networks," *AIAA Journal of Spacecraft and Rockets*, submitted for publication.

16. A. M. Baker, A. da Silva Curiel, T. Vladimirova, C. P. Bridges, and D. J. Barnhart, "Thinking Outside the Cube: A Radical New Approach to Nanosatellite Missions," *Proceedings of the 59th Int. Astronautical Congress*, Glasgow, 2008, to be published.

Other publications supported during this research:

17. D. J. Barnhart, J. J. Sellers, C. A. Bishop, J. R. Gossner, J. J. White, and J. B. Clark, "EyasSat: A Revolution in Teaching and Learning Space Systems Engineering," in *Proc. AIAA Space Systems Engineering Conf.*, Atlanta, GA, November 2005.
18. D. J. Barnhart, T. Vladimirova, A. Ellery, V. J. Lappas, C. I. Underwood, and M. N. Sweeting, "Utilising the EyasSat Concept in Space Systems Engineering Courses at the University of Surrey," in *Proc. 57th Int. Astronautical Congress*, Valencia, Spain, 2006, Paper IAC-06-E1.4.04.
19. P. Swan, J. Sellers, and D. J. Barnhart, "Teaching Space Systems Verification and Validation Using EyasSat–Adding Reality," in *Proc. 58th Int. Astronautical Congress*, Hyderabad, India, 2007, Paper IAC-07-D1.1.10.
20. T. J. Lawrence, D. J. Barnhart, L. M. Sauter, F. T. Kiley, and K. E. Siegenthaler, "The United States Air Force Academy FalconSAT Small Satellite Program," in *Small Satellites: Past, Present, and Future*, H. Helvajian, Ed. Reston, VA: AIAA Press, 2008.

1.5 Research Impact

During the course of this research, progress reported in the publications just listed has helped renew an interest in very small satellites, which have largely been dismissed as academic curiosities. The following activities have been directly influenced by the outcome of this work:

- The heterogeneous system-on-a-chip design part of this research is largely supported by a grant from the European Office of Aerospace Research and Development (EOARD) of the U.S. Air Force Research Laboratory, who have provided a positive feedback on the results.
- Results of this research are included in a joint SSC/SSTL research effort funded by ESA titled, "Wireless Sensor Motes for Onboard Networking and Inter-satellite Communications," which has been very well received by ESA.
- In a collaborative effort with the USAF Academy, a constellation of PCBSats has been selected by the USAF Space Test Program at NASA's Johnson Space Center for a launch on the Space Shuttle (STS-131) first quarter 2010. Funding sources are currently being sought for the unprecedented low mission hardware cost of $264,590, which includes a constellation of 10 satellites and ground station. The mission is the case study proposed in this research.
- A single PCBSat has been selected as a static payload on the International Space Station MISSE-7 experiment package, due for launch first quarter 2009. The purpose of this flight is on-orbit validation of the commercial components.

1.6 Structure of Thesis

The structure of this thesis is organized as follows:

Chapter 2 presents the state-of-the-art in the areas of distributed missions, systems, very small satellite technologies, and wireless sensor networks. The purpose of this chapter is to identify fundamental user-driven problems and potential solutions for investigation in this research. Secondly, it clearly shows how this research builds on the existing contributions in this field.

Chapter 3 discusses a range of meaningful distributed science missions and supporting miniature payload sensors. A case study mission investigating ionospheric plasma depletions is presented. The basic mission architecture and requirements are defined which drive the development and comparison of very small satellite technologies discussed throughout this research.

Chapter 4 presents the feasibility assessment of a monolithic system-on-a-chip design approach to satellite miniaturisation, which is called *SpaceChip* in this work. SpaceChip proves to be more widely applicable than originally thought, supporting wireless sensor network architectures in hostile environments where ultra-light sensor nodes are required. Furthermore, the chapter concludes with an assessment of the required technologies to support the design approach.

Chapter 5 focuses on the development, simulation, and hardware test results of two key subsystems for environmentally tolerant heterogeneous system-on-a-chip (SoC) applications. A new technique that enables monolithic photovoltaic power supplies is presented. Secondly, an environmentally tolerant microprocessor design methodology is discussed.

Chapter 6 introduces the *PCBSat* design approach, which is an investigation of developing the smallest practical satellite entirely from existing commercial off-the-shelf (COTS) components and fabrication technologies with a focus on low cost. A detailed treatment of a prototype flight model design and fabrication techniques is presented.

Chapter 7 reports on the characterisation and test results of the PCBSat flight model, targeted for the case study mission. Functional and environmental results are included.

Chapter 8 proposes an initial assessment of the cost effectiveness of all very small satellite design approaches considered in this research. Availible power and payload volume are used as the baseline metrics for comparing all technologies with a focus on massively distributed scenarios.

Chapter 9 concludes the research, clearly identifying the novelty and impact of the key contributions of this work to the state-of-the-art. Potential follow-on efforts are proposed to advance the ideas presented in this research.

Chapter 2

2 Literature Review

This chapter reviews previous work relevant to this body of research. The review is presented in a problem–solution format, where unanswered fundamental user-driven missions can be solved by very small satellites, which is the underlying motivation of this research. Distributed space missions are first discussed and classified in Section 2.2, highlighting the high cost of these systems, concluding with stymied missions that can be enabled by space sensor networks. An overview is given in Section 2.3 of potentially applicable very small satellite technologies. Terrestrial wireless sensor networks are then discussed in Section 2.4, suggesting that this technology can be applied to the space environment. Section 2.1 first gives a brief chronology of enabling developments.

2.1 Introduction

During the first 50 years of the space age, space system architectures have rapidly transformed from short-lived single-spacecraft missions to distributed satellite systems. Concurrently, individual satellite mass has grown from Sputnik's 84 kg to beyond 6000 kg in some cases. However, there is a growing trend towards constellations of smaller satellites to provide new distributed sensing capabilities. Terrestrial wireless sensor networks have also flourished during this time, mirroring the trend in new distributed sensing applications. An approximate timeline is presented in Table 2-1 highlighting the significant milestones that directly enable this research.

Table 2-1. Approximate Timeline of Enabling Technologies

1800's	Artificial satellites proposed
1945	Global satellite communication system proposed
1957	First satellite launched
1978	First distributed satellite system launched (GPS)
1992	Smart Dust and wireless sensor network concepts proposed
1993	Silicon satellites, satellite-on-a-wafer proposed
1994	Satellite-on-a-chip envisaged
1995	Satellite formation flying proposed
1996	Distributed satellite systems discussed widely
1998	Smart Dust wireless sensor nodes developed from multi-chip modules
1999	New mass-producible spacecraft concepts emerge
2000	First sub-kilogram satellites launched and CubeSat standard proposed
2004	Spacecraft fractionation proposed

2.2 Distributed Space Missions

The interchangeable terms, *distributed satellite system* and *distributed space system*, evoke the promise of realizing missions that have not been previously possible, whilst the term *constellation* is typically associated with a historical implementation of the concept. Jilla [4] defines a distributed satellite system as "a system of multiple satellites designed to work in a coordinated fashion to perform a mission." Burns [5] expands the definition to "an end-to-end system including two or more space vehicles and a cooperative infrastructure for science measurement, data acquisition, processing, analysis, and distribution." Shaw [6] offers the most complete definition, identifying two formal types. The first relates to system implementations where multiple satellites are sparsely distributed in a traditional constellation to meet mission requirements. Constellation scenarios do not typically require precise orientation between spacecraft but may optionally require propulsive stationkeeping. Satellites in a constellation are linked via ground relays and systems, with the rare exception of crosslinks or inter-satellite links.

The second distributed satellite system type classified by Shaw introduces the concept of a local *cluster*, where satellites are intentionally placed close together in nearby orbits to train on a common target. Optionally, this cluster of satellite nodes may have a more complex instantiation, frequently referred to as a *formation*. *Formation flying* requires that satellites in a cluster maintain precise spacing and orientation relative to each other, with the level of precision based on mission requirements. This requirement directly implies that the spacecraft must have exact real-time location knowledge of all nodes and a propulsion system to maintain the formation. An ideally placed formation can only briefly exist before orbital perturbations disturb the arrangement. The motivation for formation flying is to synthesize a virtual aperture, antenna, or other sensor to attain mission performance levels that currently cannot be achieved by a monolithic satellite. Many aspects of this concept have been widely studied, but the first active mission has yet to be realized, with the exception of a few initial experiments discussed later in Section 2.2.2.5.

A distributed satellite system taxonomy is proposed in Figure 2-1 based on their predominant characteristics. However, it is not to be taken as mutually exclusive. For example, a formation-flying cluster inherently requires crosslinks. The term *swarm*, which is frequently used in the literature without agreement, is not included in this classification diagram. The opinion of the author is that it best describes a natural phenomenon of a random nature, which is not practically achievable on orbit. Current and future distributed missions are presented next categorically. All mission costs given are based on the best available public mission announcements.

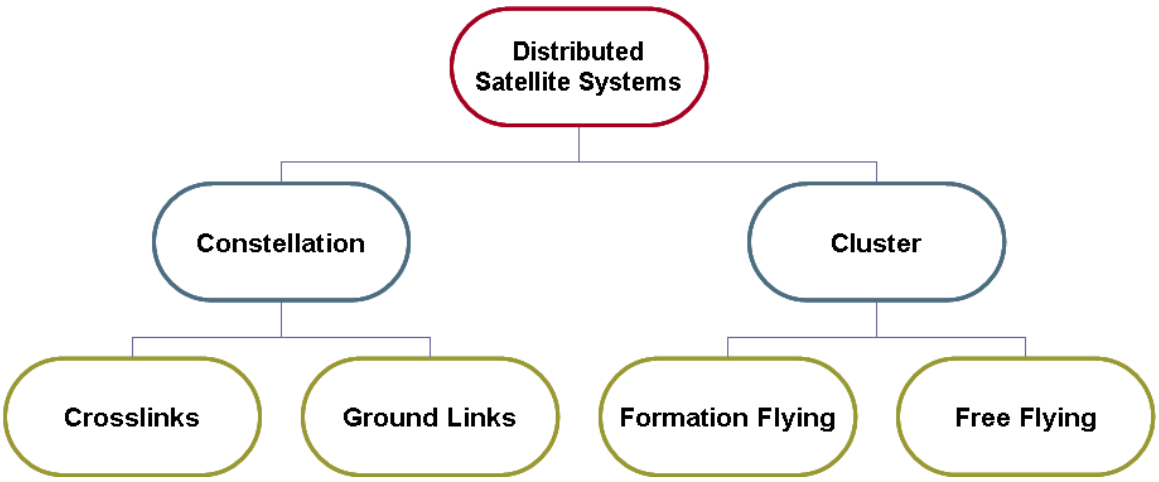

Figure 2-1. Distributed Satellite Systems Taxonomy

2.2.1 Current Distributed Space Missions

Table 2-2 presents a selection of current distributed satellite systems grouped in the four typical mission categories, which also serves to outline the discussion in this section. The first, largest, and best example of a distributed communications system is the $5 billion IRIDIUM global mobile telephone network launched in 1997 [7]. Globalstar is a similar system with near-global coverage. ORBCOMM offers near-global paging and messaging services.

Table 2-2. Selected Distributed Satellite Systems

Mission Type	System	First Launch	Number of Satellites	Orbit	Satellite Mass (kg)	System Cost (Million USD)
Communication	IRIDIUM	1997	66	LEO	689	~5,000
	Globalstar	1998	24	LEO	222	unknown
	ORBCOMM	1997	29	LEO	42	~330
Navigation	GPS	1978	24	MEO	989-1,077	>2,000
	GLONASS	1982	24	MEO	~1,400	unknown
Remote Sensing Science	DMC	2002	5	LEO	166	40
	EOS	1997	17	Varied	Varied	unknown
	Cluster/DS	2000	6	HEO	1,200/330	~600
	ST5	2006	3	MEO	25	130
	COSMIC	2006	6	LEO	69	55
	THEMIS	2007	5	HEO	128	200

GPS, GLONASS, and the proposed European Union's (EU) Galileo system are traditional constellations with ground links. The GPS constellation is composed of 24 satellites in semisynchronous medium-Earth orbits (MEO), placed evenly in six planes to provide position and timing information to users on land, sea, air, and space.

Small satellites have recently entered the Earth observation market. For example, the Disaster Monitoring Constellation (DMC) is the first commercial Earth imaging constellation [8]. It offers

an unprecedented revisit time of 24 hours, versus days or weeks available from other systems, without crosslinks but through a network of strategically placed groundstations.

The Cluster and Double Star (DS) mission, launched in 2000, is arguably the first satellite cluster of six satellites to gather scientific data on the magnetosphere in three dimensions [9]. Similarly, the Earth Observation System (EOS) is a coordinated collection of 17 satellites performing various types of remote sensing and science missions. The recent launches of ST5, FORMOSAT-3/COSMIC, and THEMIS indicate a growing interest in distributed science missions.

The next four sections discuss these missions in more detail, including some basic discussion of the associated orbital mechanics. Emerging missions are then presented categorically.

2.2.1.1 Current Distributed Communication Missions

Communication missions are generally realized using Geostationary (GEO), Molniya, or LEO constellations presented by Wertz to connect two or more users on the ground [10]. Near-global coverage missions, excluding very high latitudes, utilize a minimum of 3 satellites evenly spaced in GEO as first proposed by Clarke [2]. GEO is achieved by placing a satellite above the equator at a distance of 42,158 km from the centre of the Earth. Satellites in this orbit appear to be at a fixed point in the sky to the user on the ground. This observation is due to the angular velocity of the satellite exactly matching that of the Earth, i.e. the orbital period equals one Earth revolution.

Wertz and Larson note the advantages of this orbit: simple constellation design, fixed small antennas on the ground, and near-global coverage using only three satellites [11]. However, the satellite will have complex pointing requirements, have a large electrical power budget to support a high radio frequency (RF) output, and require constant orbit maintenance to maintain position. In addition, there is a noticeable signal delay when using this system for real-time voice communications due to the distances involved, especially in multi-hop scenarios.

Many global voice/data services utilize this type of constellation. The $2 billion Inmarsat-4 constellation of four satellites is a good example of a commercial system, whilst the $10 billion MILSTAR constellation of four satellites is an example of a military system. Most GEO communication constellations are considered distributed space mission constellations with ground links, with the exception of MILSTAR, which has crosslinks. Crosslinks were first seriously investigated by Solman, but are not yet widely used [12].

Regional coverage at mid to low latitudes can be realized by placing a single satellite on the equator near the region where coverage is desired. In Europe, the Sky system delivers television whilst WorldSpace delivers radio programming. Over the U.S., the DirecTV and DISH systems deliver television, whilst radio services are offered by XM and Sirius. These systems are arguably considered distributed missions, as they collectively employ multiple satellites.

Regional coverage at high latitudes can be obtained with at least two satellites operating in a Molniya (Russian for lightning) orbit. These orbits are specially designed to leverage an orbital perturbation created by the Earth's oblateness (i.e. imperfect sphere). At an exact inclination of 63.4 degrees, a period of 12 hours, and an elliptical shape, the orbit produces a repeating ground track with a unique quality. The satellite appears to "hover" over two separate points on the Earth for 11 hours over each spot and a "lightning fast" (30-minute) shift in between.

Molniya orbits enable only two satellites to provide near-continuous coverage of a region (including Polar regions) and reduce launch costs due to the lower orbit insertion requirements. Consequently, users have non-trivial antenna pointing requirements, small gaps in coverage unless three satellites are used, and the satellite's pointing and transmit power requirements will still be high. Many amateur radio, communication, and military satellites use this type of orbit.

Truly global coverage with no user antenna pointing requirements or significant signal delays can be realized in LEO with a constellation composed of a large number of satellites. LEO begins at the lowest possible altitude where orbit can be sustained for a short amount of time, typically around 130 km up to about 1000 km, although there is no universal definition where LEO ends.

LEO offers several advantages. The radiation environment is fairly benign, with the exception of single event phenomena. Satellites at this altitude can have an impressive optical resolution and require less RF power for communication links. A propulsion subsystem with a significant amount of fuel is required to maintain orbit, due to the extended drag effect of the upper atmosphere. Another disadvantage is that satellites in LEO are visible to ground stations and observers for only a dozen or so minutes at a time compared to longer times at higher orbits.

Garrison [7] summarizes the first, largest, and best example to date of a constellation utilising crosslinks: the $5 billion IRIDIUM global mobile phone communications system first launched in 1997. IRIDIUM employs a nominal constellation of 66 satellites, each weighing 689 kg, which provides global telecommunications services with very low latency to users with compact handsets. IRIDIUM is also one of the first distributed systems with some degree of autonomy.

Peters focuses on the fact that IRIDIUM is the only commercial system to date that employs RF crosslinks [13]. Although the advantages of crosslinks are well known, their cost and complexity have discouraged any new systems from being fielded. As mentioned previously, the MILSTAR system is the only military system currently using RF crosslinks. Optical crosslinks are being considered for future missions.

In the 1990's a boom of commercial data services based on large LEO constellations was predicted as discussed by Ashford [14]. The only other global telecommunications systems that have been fielded are the $4 billion Globalstar constellation of 48 satellites, providing satellite telephone coverage over populated continental regions and ORBCOMM, which provides low data

rate messaging and tracking services. The visionaries behind these systems did not foresee the rapid expansion of terrestrial mobile wireless services and subsequently experienced bankruptcy and restructuring [15]. However, new applications are emerging for these constellations, which have encouraged investors to replenish them over the next decade [16].

2.2.1.2 Current Distributed Navigation Missions

All three navigation systems discussed here are constellations utilising ground links. The GPS constellation is composed of 24 satellites in semi-synchronous orbits, placed evenly in six planes designed to provide position and timing information to users on land, sea, air, and now space [17]. The system costs at least $400 million annually to operate and sustain.

Semi-synchronous orbits have a period of exactly 12 hours. The orbit is usually circular in shape and inclined from the equator to achieve global coverage. The main advantage of this orbit is that it produces a repeating ground track on the surface of the Earth. The main disadvantage of this orbit is that it places the satellite in the Van Allen radiation belts.

Russia operates a similar system called GLONASS that utilizes 12 to 14 satellites in two planes. They have recently announced future upgrades to the system. In 2005, the EU funded and launched the $40 million, 660 kg GIOVE-A technology pathfinder mission to support technology development for Galileo [18]. Its future is not certain, as EU member states continue to debate the priority of funding the system, considering there are two existing systems already.

2.2.1.3 Current Distributed Remote Sensing Missions

Remote sensing missions encompass a wide variety of specific missions operating over the full electromagnetic spectrum. Tradeoffs in remote sensing constellation design mirror communication missions where size and altitude determine coverage and performance.

The ideal orbit for Earth observation or imaging missions is the sun-synchronous orbit. A sun-synchronous orbit is achieved at an interrelated altitude and inclination in LEO that causes the orbit to precess about one degree per day, leveraging the same perturbation used by Molniya orbits. The result is that the orbit maintains the same orientation with the sun all year long, producing similar lighting conditions and revisit times each day. The characteristics of the orbit are similar to others in LEO.

Civil and military meteorological missions utilize satellites operating in sun-synchronous orbits, such as TIROS-N and DMSP. A view from GEO is also needed, which come from systems such as GOES and METEOSAT. They accomplish this mission by carrying visible, ultraviolet (UV), and/or infrared (IR) imagers. These multiple-satellite systems are simple constellations with ground links.

Commercial imagery applications where satellites take visible and IR images of specific regions of interest in the world are also widespread. Commercial imagery is used for mapping, agricultural data, disaster monitoring, and other requirements. Systems such as QuickBird, OrbView, IKONOS, SPOT, and Landsat offer resolutions up to 0.6 metres. It should be noted that none of these satellites originated within the context of a distributed system. Recent consolidation in the industry has enabled the claim of a new imaging constellation.

Small satellites have recently entered the Earth observation market. The DMC, composed of five, 166 kg, $10 million Earth-imaging satellites, offers an unprecedented revisit time of 24 hours, versus days or weeks when compared to the other commercial and government imaging systems [8]. The DMC is considered the first Earth imaging constellation.

2.2.1.4 Current Distributed Science and Exploration Missions

Science and space exploration missions are generally considered as a single mission area, but each mission is unique with its own specific requirements. These mission areas are typically under great financial constraint and usually manage single satellites, interplanetary probes, or payloads that ride secondary to another system [19]. Recently, new interest has developed in scientific constellations; however, none of them yet employs crosslinks.

The National Aeronautics and Space Administration's (NASA's) EOS represents the coordination of 17 satellites performing various types of remote sensing and science missions with its international partners, including the European Space Agency (ESA). The segment of EOS most interesting to this research is referred to as the *A-train*, which is a set of six satellites in the same 705 km sun-synchronous orbit. Of those, PARASOL, CALIPSO, CloudSat, and Aqua are closely spaced, with the smallest distance being 100 km between CALIPSO and CloudSat [20].

Cluster is a maintained constellation of four 1,200 kg satellites that forms a tetrahedron of various geometries on a periodic basis [9]. Two additional Double Star satellites, with a mass of 330 kg, allow simultaneous sensing up to six points. Launched in 2000, it is arguably the first satellite cluster to gather scientific data on the magnetosphere in three dimensions.

The $140 million ST5 program [21], launched in 2006, is a part of NASA's New Millennium Program. The three-satellite constellation, each with a mass of 25 kg, was designed to evaluate technologies that can be used in future missions, mainly for space weather. Fong [22] presents the $60 million FORMOSAT-3/COSMIC (Constellation Observing System for Meteorology, Ionosphere, and Climate) program launched in 2006. COSMIC is a constellation of six 69 kg satellites.

2.2.2 Emerging Distributed Space Missions

Since 1995, there has been a significant increase of distributed mission works. For example, the terms *distributed satellite systems*, *satellite formation flying*, and *satellite cluster* have become prevalent in publications of the American Institute of Aeronautics and Astronautics (AIAA) as highlighted in Figure 2-2. Before 1995, *satellite cluster* describes close spacing in GEO.

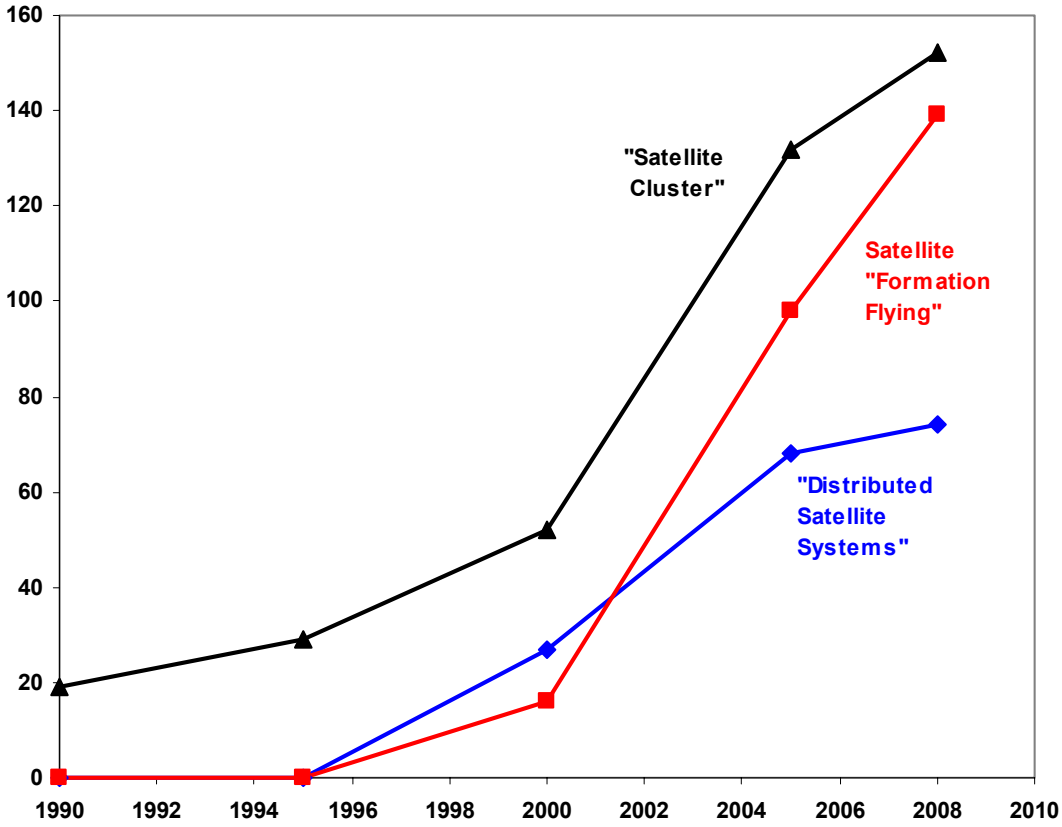

Figure 2-2. Notable Publication Surge in Distributed Mission Topics Published by AIAA

2.2.2.1 Emerging Distributed Communication Missions

Considering communication missions first, recall that Ashford [14] noted current realities fall short of previous predictions of a LEO communications system boom. For example, a large-scale system that never materialized was Teledesic, backed by Microsoft. With conceptual designs ranging up to 840 satellites costing $5 million each, Teledesic was to provide the first global wireless internet. The Teledesic mission was abandoned after witnessing the technical successes and economic struggles of the IRIDIUM, Globalstar, and ORBCOMM constellations. Norris [23] has proposed that clusters of small satellites operating in LEO will eventually compete with larger ones in GEO. This may become reality as the GEO belt fills up, especially over the most populated areas of the Earth. Another variant of this idea, put forth by Edery-Guirardo [24] is to augment larger satellite missions with a constellation of smaller communication relay satellites.

2.2.2.2 Emerging Distributed Navigation Missions

GPS, GLONASS, and the up and coming Galileo mission have already been categorized as constellations using ground links. Crosslinks have been proposed for GPS III [25], but to date, no one has proposed clusters for distributed navigation systems. Instead, the current focus is on their vulnerability to jamming. For GPS in particular, next generation systems will mitigate this vulnerability with the combination of higher power RF signals and other anti-jam technologies causing the satellite mass to rise from 1,000 kg now to over 1,500 kg. The threat of jamming will likely grow, requiring larger systems with increased RF power.

2.2.2.3 Emerging Distributed Remote Sensing Missions

There are numerous envisaged distributed remote sensing systems, yet very few of them have gone beyond the conceptual or experimental phase. A short list of constellation-based mission examples is presented, which require distributed or multi-point sensing:

- Natural disaster pre-emptive warning and detection
- Environmental treaty monitoring, such as Kyoto Protocol or RF spectrum management
- Space situational awareness, signals intelligence, and other military missions [26]
- Constellation sharing where contributing members access the services of the entire group
- Deployable satellite inspectors for local electromagnetic field measurements [27]
- In particular imaging with frequent temporal repeats and high spatial resolution
- On-demand real-time imaging of any location on Earth
- Beam forming to remotely sense a particular location at optical or radio wavelengths

2.2.2.4 Emerging Distributed Science and Exploration Missions

Science and exploration missions have traditionally been dominated by single-spacecraft or interplanetary probe architectures due to typically limited science budgets and resources. New distributed sensing missions are being considered based on small satellites, such as:

- Disposable rapid-response sensor networks for use in LEO and the upper atmosphere
- Magnetotail behavioural studies, including ion and electron scale space weather events, solar wind variations, and other Geospace science [28]
- Deployable satellites for enhanced Earth magnetic field measurements [29]
- Interplanetary exploration based on satellite-on-a-chip, smart dust, wireless sensor networks, and networked electronic cubes [30]-[31]

- Detailed characterisation of environments to support interplanetary exploration, such as Mars, asteroids, or other planets [32]
- Monitoring wide-area highly time dependent phenomena, such as atmospheric drag, ionospheric plasma, or Aurora in LEO [33]-[35]
- Sensor web of terrestrial and space-based systems [36]
- Very small satellite-based science missions for space weather and atmospheric research [37]

2.2.2.5 Emerging Space System Architectures

All of the missions discussed so far are based on traditional constellations, although some may require unusually large numbers of measurement points. One emerging system architecture is *formation flying* of a cluster of satellites, pioneered by the Aerospace Corporation in 1995 [38]-[39]. Formation flying proposes that satellites maintain a fixed orientation and distance, from hundreds of kilometres to picometer spacing, to synthesize a larger electromagnetic aperture than is possible with a single monolithic satellite. TechSat 21, with a space-based radar mission, was one of the first widely discussed implementations of formation flying [40].

The Terrestrial Planet Finder mission is a serious formation-flying proposal for science and exploration that is currently under study [41]. This mission will employ a formation flying cluster at one of the Sun-Earth libration points to synthesize a very large aperture to see further in the universe than any existing system. Bristow is one of the first to outline some of the future formation flying missions [42]:

- Space sensor webs
- Earth applications—radar, signals interferometry, sentinels
- Earth space environment—mapping of radiation belts, magnetosphere, gravity field
- Earth science—climate, ionosphere, aurora, precipitation, vegetation, land and sea condition
- Astronomy—full spectrum interferometry, planet finder

Bristow [42] also summarizes the challenges associated with formation flight. It is a very complex, multi-faceted problem involving mission architecture, hardware, and software:

- Formation design—mission specific, centralized/decentralized architecture, payloads
- Communications—architecture, planning, scheduling, robust fault-tolerance
- Data handling—energy-optimized operations, autonomous control algorithms
- Subsystems—efficient propulsion, actuators, guidance, navigation and control sensors, optical/RF ranging, computing capacity

Due to the complexity of a formation flying system architecture, no complete formation flying missions have been implemented beyond a few initial experiments. NASA conducted a formation flying experiment with Landsat and Earth Observing 1 (EO-1) in 2001 [43]. A semi-autonomous formation control algorithm on EO-1 using its own GPS position data and uploaded Landsat position data was successfully demonstrated. Eventually, fully autonomous systems onboard spacecraft with their own position determination ability will close the loop. The Orion-Emerald mission was proposed as a purpose-built formation-flying demonstration but the mission never materialized [44]-[45].

Finally, s*pacecraft fractionation* is the idea that large monolithic satellites can be broken into key components contained in small satellites orbiting as a free-flying cluster, wirelessly networked together. The concept originated with the fault-tolerant and distributed nature of formations [38]-[39]. As formation flying has not yet materialized as quickly as envisaged, many of its qualities have been applied to meet new requirements regarding the responsiveness of space assets to new technologies and threats [46]-[48]. The U.S. Defense Advanced Research Projects Agency (DARPA) recently provided $38 million in funding to four competing teams to develop the *F6* demonstration mission (Future Fast, Flexible, Fractionated, Free-Flying Spacecraft united by Information eXchange) [49]. This type of system architecture allows for component upgrades without the complexity of physical servicing. The system architecture proposes a free-flying cluster of satellites [50] and specifically avoids formation flying discussions. However, it is conceivable that many of the technologies to be developed as shown in Figure 2-3 [51] could support future formation flying missions.

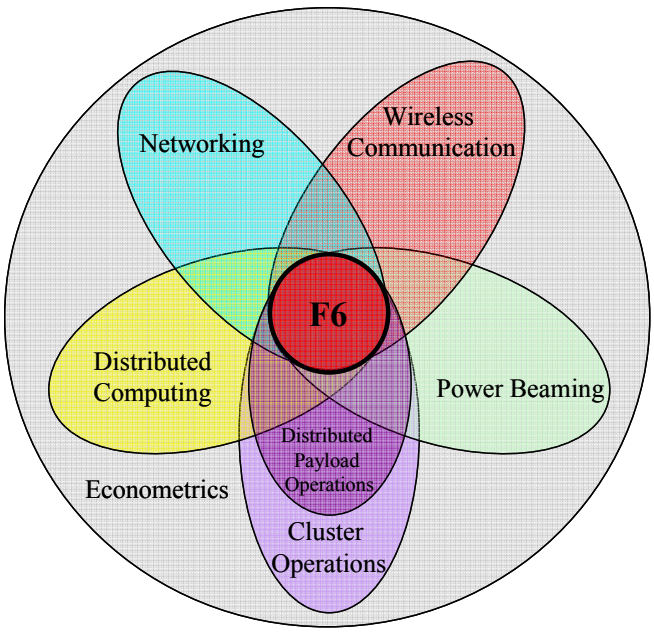

Figure 2-3. Spacecraft Fractionation Technology Enablers [51]

2.3 Very Small Satellite Technologies

As presented in Chapter 1, increasing mission requirements have driven up satellite mass from Sputnik's 84 kg in 1957 to over 6,000 kg in 2007. Consequently, cost, complexity, program timelines, and management overhead have grown considerably. Countering this trend, the small satellite movement with its academic beginnings is now a fast-growing industry. Leveraging commercial technology and focusing on low-budget, high-impact missions with achievable goals, small satellites, defined as having a mass below 500 kg, have been widely demonstrated with respectable capabilities.

The space community generally agrees on the mass classification shown in Figure 2-4. The satellites in italics, such as *GPS*, have been developed elsewhere, whilst the rest have been developed by the University of Surrey through its commercial spinoff, Surrey Satellite Technology, Ltd. (SSTL). Approximate mission costs are also listed, noting at the time of publication, one Great Britain Pound (GPB) is worth approximately two United States Dollars (USD) (£1 ≈ $2). The frequency of small satellite launches is illustrated in Figure 2-5 [52]. Note the preponderance of missions is in the microsatellite and minisatellite categories.

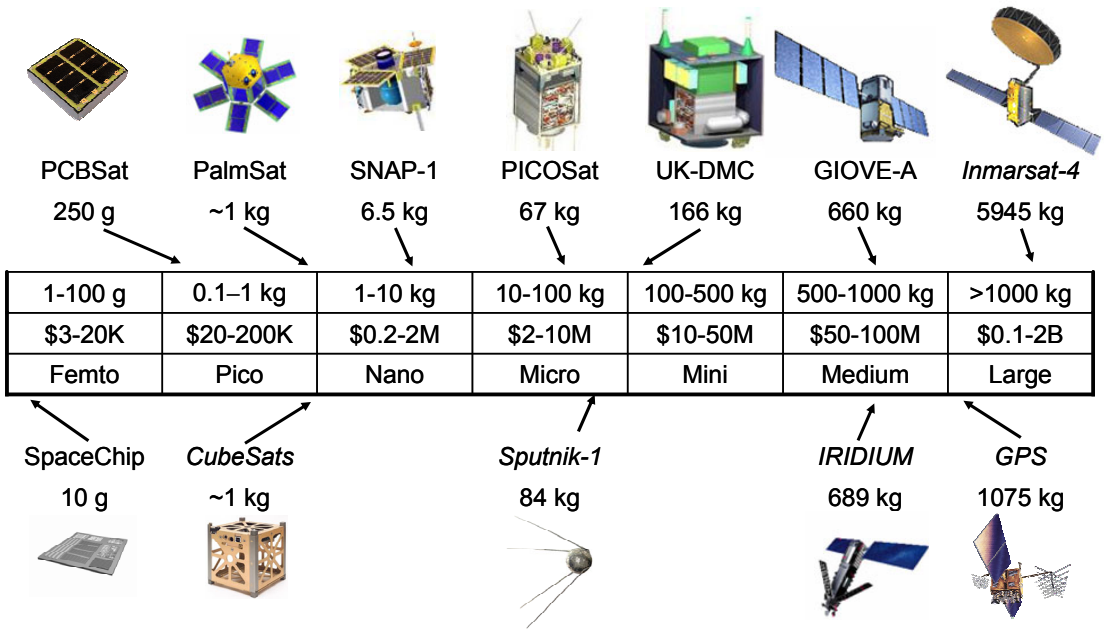

Figure 2-4. Satellite Mass and Cost Classification

The major challenge for implementing the equivalent of a wireless sensor network in space using very small satellites is twofold. The unique environment presents complex orbital dynamics with non-ideal perturbations and hazardous conditions, including the upper atmosphere, debris, vacuum, radiation, and launch. Secondly, the sub-kilogram constraint greatly limits the selection of miniature payloads, electrical power generation, communication range, and propulsion capabilities.

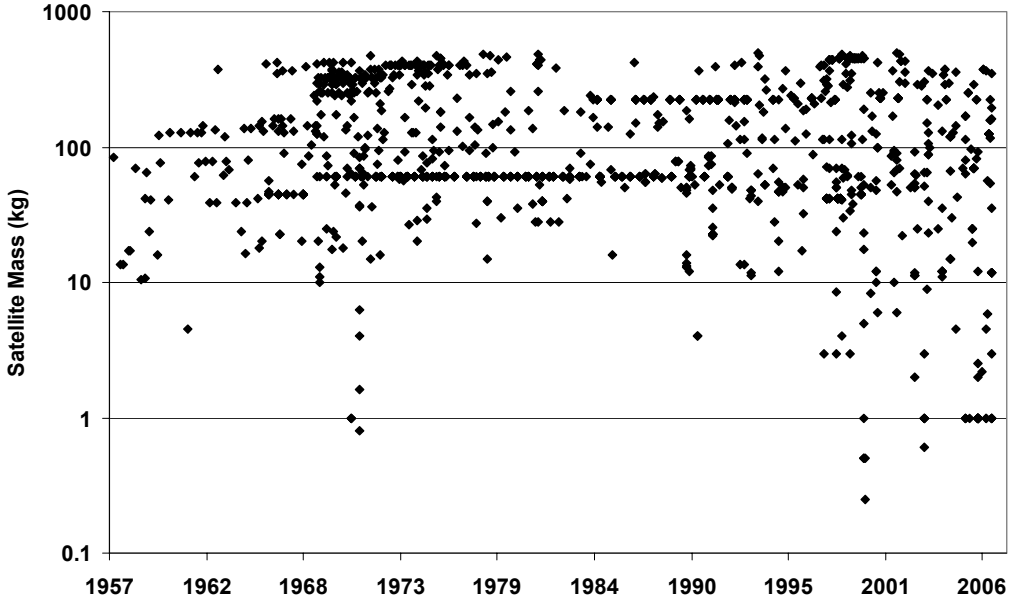

Figure 2-5. Small Satellite Histogram [52]

2.3.1 Current Very Small Satellite Technologies

Although minisatellites and microsatellites clearly dominate small satellite missions, this research is focused on looking at the downward trend from nanosatellites to femtosatellites. A launch history of these mission categories is given in Figure 2-6, which is a subset of Figure 2-5. The missions in the 1960's and 70's are mainly calibration spheres, whilst the missions focused on demonstrating advanced satellite miniaturisation began in 2000.

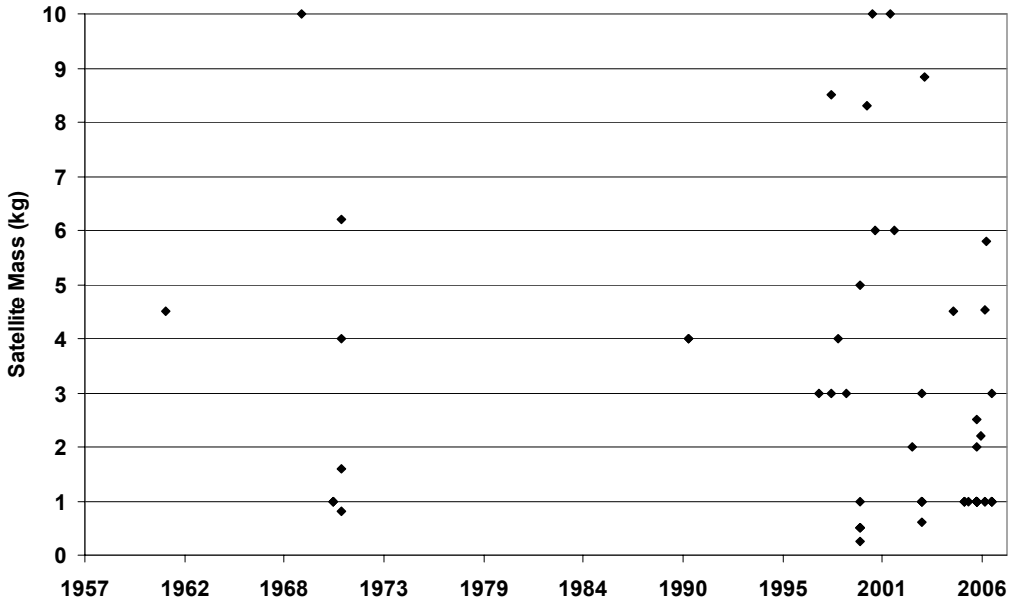

Figure 2-6. Mass Histogram of Nanosatellites and Picosatellites [52]

2.3.1.1 Nanosatellites

Microsatellites are generally regarded as the smallest satellite platform from which meaningful missions can be performed. This is primarily due to the surface area available for power generation, the internal payload volume, and the ability to provide propulsion. Over a dozen nanosatellites have flown in the past 15 years, mostly focused on science or academic missions, including the six 1.5 kg MEPSI series, the 3 kg RAFT, and the 4 kg MARScom satellites, all with a primary purpose of supporting satellite tracking studies.

The $2 million, 6.5 kg SNAP-1 mission launched in 2000, is considered the first nanosatellite to demonstrate the complete set of satellite functions typically found in larger satellites, including full attitude and orbit determination and control [53]. SNAP-1 was built primarily with COTS components at the University of Surrey, Surrey Space Centre (SSC). SNAP-1 demonstrated spacecraft inspection and wide area earth imaging. SNAP-1, shown in the foreground of Figure 2-7, also attempted formation flying with the co-deployed Tsinghua-1 microsatellite, shown in the background. Although nanosatellites are not considered very small satellites in this research, it is important to appreciate the capabilities of this nearest neighbouring category [54].

Figure 2-7. SNAP-1 Nanosatellite [53]

MicroLink-1, originally developed as NanoSpace-1, is an ongoing effort by Ångstrom Aerospace Corporation to develop a more capable nanosatellite than SNAP-1 [55]-[56]. The mission of MicroLink-1, with a mass up to 10 kg, is to demonstrate a proprietary multifunctional module concept as shown in Figure 2-8 (left), in addition to providing a platform for on-orbit validation of flight hardware. Their stated goal is to produce nanosatellites that have the capability of present-day microsatellites. In 2006, they initiated a collaboration with the CANEUS Nano-Pico-Satellite consortium. The consortium claimed that within three years, they could mass produce very capable nanosatellites for $4 million and picosatellites for $2 million [57].

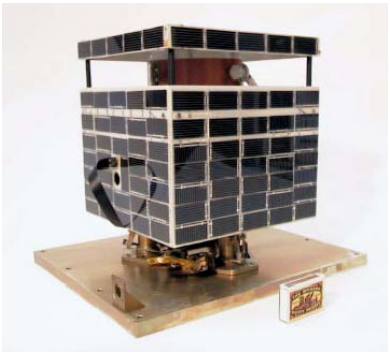

Figure 2-8. MicroLink-1 Concept (left) [56] and Munin (right) Nanosatellites [58]

Another notable nanosatellite concept is a space weather monitoring constellation of nanosatellites [58]. The ESA proposal suggests that COTS-based nanosatellites, such as the 6 kg Munin shown in Figure 2-8 (right) and flown in 2000, could be used to monitor and aid in forecasting space weather phenomenon. ESA has continued to fund this effort, with the next phase just completed in April 2008. The report is not yet publically available.

One of the smallest nanosatellites in development is PalmSat, which currently supports space systems engineering education at the University of Surrey. PalmSat is the next evolutionary step in miniaturisation from SNAP-1 [59]-[60]. Similar to SNAP-1, the mission of PalmSat is to demonstrate complete satellite functionality at nearly one kilogram using all COTS components. Recent estimates suggest that this can be accomplished with a mass of 1.5 kg and solar power generation of 2-3 W. PalmSat is aimed at single-ship science and experimental missions, with the potential of supporting distributed missions with intersatellite links.

2.3.1.2 Picosatellites

Satellite concepts with a mass under one kilogram is the focus of this research. Twenty three picosatellites have flown since 2000 as summarized in Table 2-3 [61]-[62]. The first five picosatellites were deployed from the 23 kg Orbiting Picosatellite Activated Launcher (OPAL) launched in 2000 on a Minotaur launch vehicle [63]. The DARPA/Aerospace Corporation Picosat 1A/1B was a tethered pair of 0.55 kg satellites as shown in Figure 2-9 (left), where the tether acted as an antenna and improved tracking. Its mission was to demonstrate the picosatellite concepts and validate miniature RF switches. The Thelma, Louise, and JAK 0.5 kg picosatellites were part of the Artemis project to study lightning [64]. The mission of the 0.23 kg Stensat picosatellite, illustrated in Figure 2-9 (right), was to serve as an amateur radio repeater. Some confusion in the literature alludes to a sixth satellite on OPAL called MASat or Hockypuck; however, this is not correct [65]. Only Picosat 1A/1B was successful, as no contact was achieved with the others. In 2001 a similar pair, Picosat 1C/1D, was ejected from the MightySat satellite after being stored on orbit for over a year, where it completed most mission objectives [66].

Table 2-3. Summary of Picosatellite Missions as of June 2008

Mission	Satellite	Bus	Deployer	Mass	Success
OPAL (2000)	Picosat 1A/1B	Custom	OPAL	0.55	Yes
	Thelma	Custom	OPAL	0.5	No
	Louise	Custom	OPAL	0.5	No
	JAK	Custom	OPAL	0.5	No
	Stensat	Custom	OPAL	0.23	No
MightySat (2001)	Picosat 1C/1D	Custom	Custom	0.55	Yes
Eurockot (2003)	AAU CubeSat	Custom CubeSat	P-POD	1	Partial
	CanX-1	Custom CubeSat	P-POD	1	No
	CubeSat XI-iV	Custom CubeSat	T-POD	1	Yes
	CUTE-I	Custom CubeSat	T-POD	1	Yes
	DTUSat	Custom CubeSat	P-POD	1	No
SSETI (2005)	CubeSat XI-V	Custom CubeSat	P-POD	1	Yes
	Ncube-2	Custom CubeSat	P-POD	1	No
	UWE-1	Custom CubeSat	P-POD	1	Yes
DNEPR (2007)	AeroCube-2	Custom CubeSat	P-POD	1	No
	CAPE1	Custom CubeSat	P-POD	1	Yes
	CP3	Custom CubeSat	P-POD	1	No
	CP4	Custom CubeSat	P-POD	1	Yes
	CSTB-1	Custom CubeSat	P-POD	1	Yes
	LIBERTAD-1	CubeSat Kit	P-POD	1	Yes
PSLV (2008)	AAUSATII	Custom CubeSat	X-POD	1	TBD
	Compass-1	Custom CubeSat	X-POD	1	TBD
	SEEDS	Custom CubeSat	X-POD	1	TBD

Figure 2-9. DARPA/Aerospace Picosat 1A/1B (left) [63] and Stensat Picosatellite (right) [64]

The seventeen remaining picosatellite missions were developed using the CubeSat educational satellite standard, defined by Stanford University and the California Polytechnic Institute [67]. CubeSat has improved the success rate of picosatellites by reducing the complexity of satellite design by standardizing the configuration and fostering a growing user support community [68]. The design concept is essentially a scaled-down version of larger satellite designs using miniaturized modules and a standard form factor of $10\times10\times N$ cm, where N can be up to 30 cm. The mass is restricted to one kilogram per 10 cm of N. One of the first CubeSats launched in 2003, CUTE-I built by the Tokyo Institute of Technology, is still operational and is shown in Figure 2-10 (left) [69].

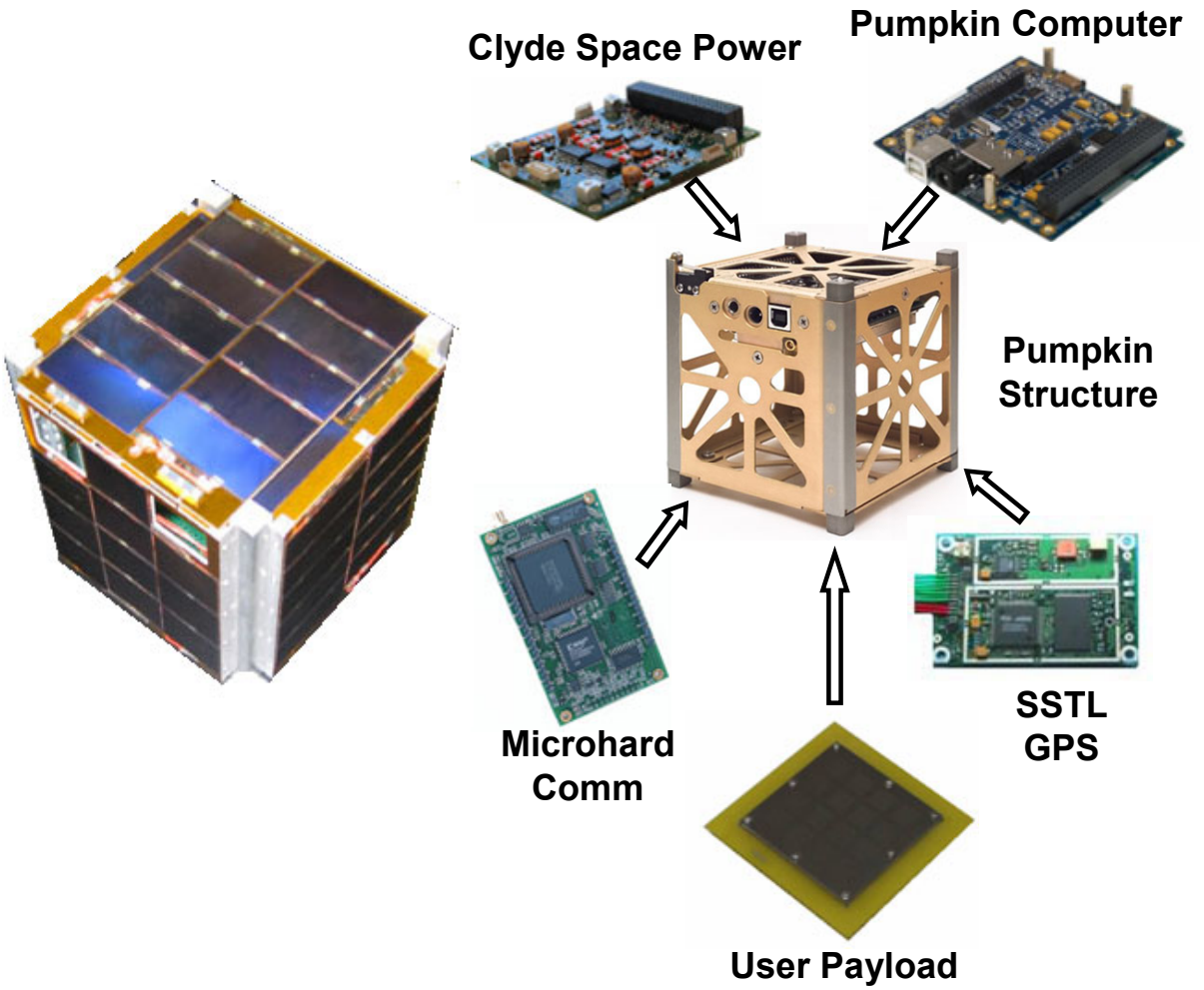

Figure 2-10. CUTE-I CubeSat [69] (left) and COTS CubeSat Concept (right) [73]-[75]

In 2003, the Eurockot launch deployed the first five sub-kilogram CubeSats, but only two were declared successful [61]. In 2005, the Student Space Exploration and Technology Initiative (SSETI) mission deployed three more sub-kilogram CubeSats from a Kosmos-3M launch vehicle, with two being successful. Unfortunately, 14 CubeSat systems were destroyed by a launch vehicle failure in July 2006 [61]. Six more sub-kilogram CubeSats were launched April 2007, with three more on 28 April 2008. Twelve new CubeSat projects were initiated in 2007 with over two dozen more in 2008 [70]. Most of these CubeSats were deployed using the Poly Picosatellite Orbital Deployer (P-POD) on a conventional launch vehicle [71]. Users in Japan, Canada, and Germany, have developed compatible deployers, such as T-POD, X-POD, and Single Picosatellite Launcher (SPL). Magnetic rail guns may be used in the future to launch very small satellites [72].

Most of the CubeSats to date have been completely custom designs using COTS components, conforming to the CubeSat standard and built by students at educational institutions. COTS subsystems have recently emerged making it possible to build a *COTS CubeSat* as illustrated in Figure 2-10 (right) [73]-[75], with the exception of a user-built payload.

2.3.1.3 Femtosatellites

The only femtosatellites to fly in space are those of the Project West Ford experiment [76]. In 1963, thousands of microgram needle-like dipoles, as illustrated in Figure 2-11, were dispersed in a successful experiment to create an orbiting relay belt for worldwide RF communications. Although the dipoles were passive, many of the concepts envisaged in this project, such as massive satellite deployment and distribution, are central to this research. More recently, Cyrospace claims to have developed a femtosatellite to support research of light bullets, but incorrectly categorized it as such with a 500 gram mass [77].

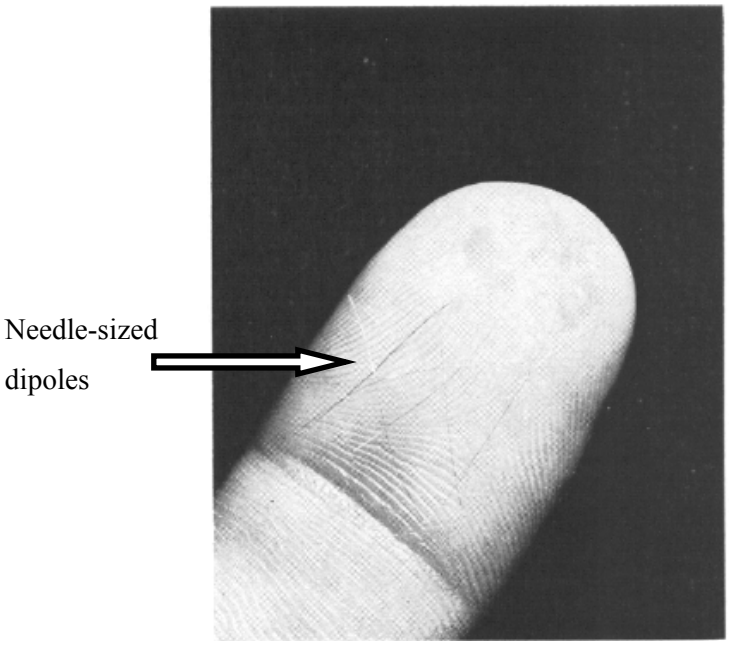

Figure 2-11. Project West Ford Femtosatellites [76]

2.3.2 Emerging Very Small Satellite Technologies

Spacecraft miniaturisation is the ubiquitous theme of the satellite industry, with the ultimate goal being monolithic integration of an entire satellite onto a single substrate, which some view as a *subsystemless satellite* [78]. Technologies presented in this section aim to enable low-cost mass-production of satellites.

2.3.2.1 Microengineered Aerospace Systems

Since 1993, Helvajian and Janson have pioneered *microengineered aerospace systems* [79]-[81]. One of their first concepts is a 500 gram *Nanosatellite*, noting that nano in this context is a reference to *nanotechnology*, instead of the now standard satellite mass classification. The terms *silicon satellite*, *satellite-on-a-wafer*, and *spacecraft-on-a-chip* emerged in these works. Integrating complementary metal-on-silicon (CMOS), which is the most common integrated

circuit (IC) fabrication technology, with microelectromechanical systems (MEMS), a more recent micro-fabrication technology, is the cornerstone of their very small satellite vision. Satellites can then be mass-produced by stacking up payloads and subsystems built entirely of silicon wafers. The concept was matured throughout the 1990's with various system configurations as depicted in Figure 2-12 [79], [82]. Xuwen [83] and later Shul [84] published similar concepts.

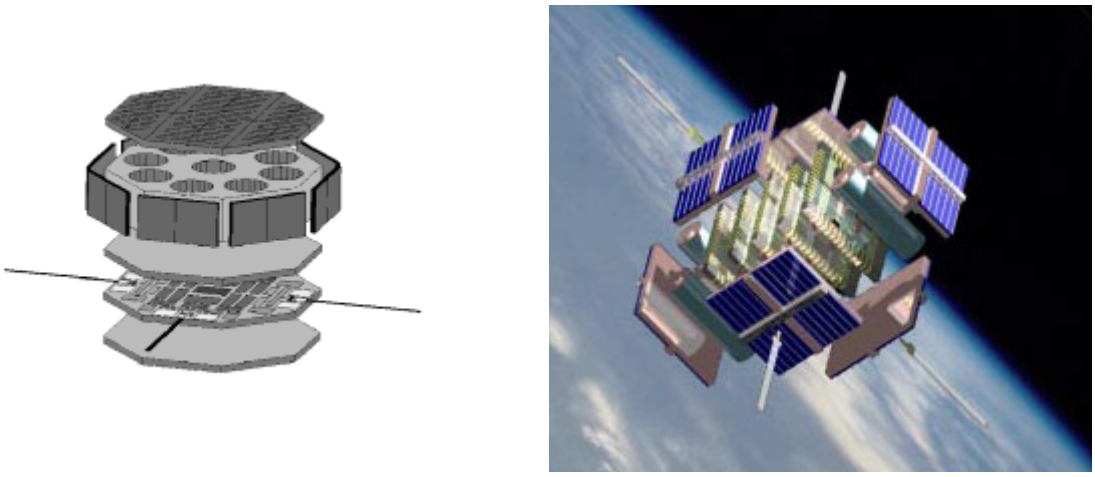

Figure 2-12. Early Microengineered Aerospace Systems Concepts [79]-[81]

In 2002, Janson and Helvajian pursued a different approach using a photostructurable glass ceramic material called Foturan™ to produce a multi-functional propulsion and structural subsystem with a focus on mass production. The Co-Orbiting Satellite Assistant (COSA) was proposed as an ejectable satellite inspector for a weeklong mission [85], having a propulsion capability (ΔV) of one meter per second. The laser-etched glass wafers of the propulsion subsystem are shown in Figure 2-13 (left) alongside the 100 gram femtosatellite (right).

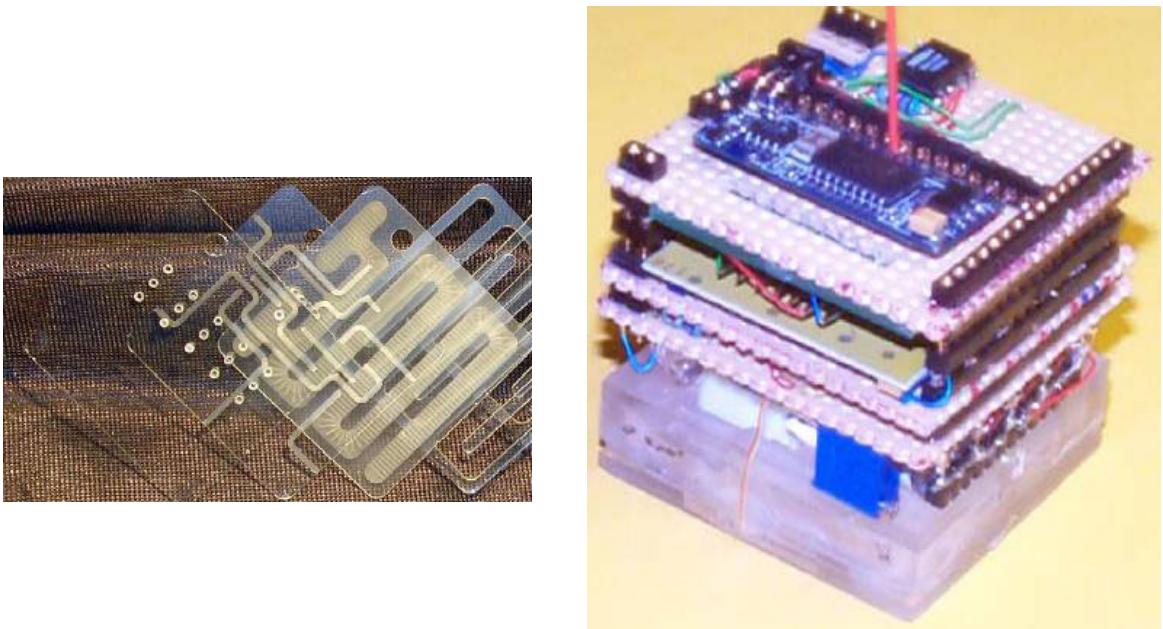

Figure 2-13. Co-Orbiting Satellite Assistant Femtosatellite [85]

COSA was revised in 2005, targeting a one-kilogram spacecraft configuration with a ΔV of 30 m/s [86]. The propulsion system, which also houses the battery, is shown in Figure 2-14 (left). A conventional PCB provides the subsystem functionality, as shown in the figure on the right. The concept was fully demonstrated on an air table.

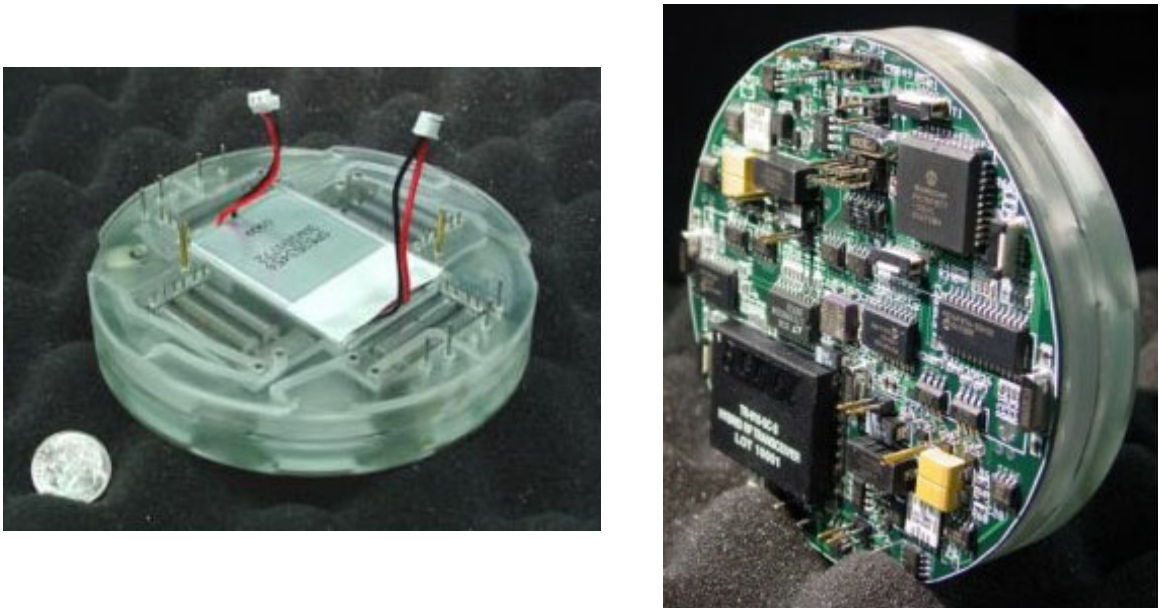

Figure 2-14. Co-Orbiting Satellite Assistant Picosatellite [86]

The concept of multifunctional structures and architectures was introduced in the same timeframe as microengineered aerospace systems, also focusing on low cost mass production of satellites [87]. The *reconfigurable multifunctional architecture* based on *multifunctional structural units* was proposed as the way forward to integrate emerging miniaturisation technologies, such as CMOS and MEMS. Bruhn [88] has taken this academic concept and intends to demonstrate it through the MicroLink-1 concept, discussed previously in Section 2.3.1.1 [55]-[56]. His proposed Multifunctional Micro Systems architecture claims to reduce satellite mass and volume by "orders of magnitude" with advanced multi-chip module (MCM) packaging technology.

2.3.2.2 Satellite-on-a-chip

Although the terms *silicon satellite*, *satellite-on-a-wafer*, and *spacecraft-on-a-chip*, were introduced in the microengineered aerospace systems effort, the first mention of *satellite-on-a-chip* can be attributed to an interview with Joshi [89] in 1994. In this research, satellite-on-a-chip is considered in the literal sense, where a complete satellite is monolithically fabricated on a single CMOS chip. Joshi [90] further proposed an *Integrated Satellite* in 1998, which is remarkably similar to Helvajian and Janson's work in 1993 [79]-[81]. Joshi applied for a U.S. patent on the concept in 1998, which was awarded in 2000 [91].

Since 1994, many have proposed satellite-on-a-chip as the ultimate goal for spacecraft miniaturisation, but very little research has been published on a specific monolithic implementation. For example, in 1995, Fleeter of Aero Astro was quoted in several articles and reports that "a $100,000 satellite-on-a-chip could be available by the end of the decade and would cost less than $50 million to develop" [92]. NASA began supporting their own concept of spacecraft-on-a-chip in 1997 through the New Millennium and Deep Space Systems Technology Programs [30], [93]. In 1999, Janson was quoted, "The goal is to one day build a satellite-on-a-chip" [94]. Panetta, NASA's nanosatellite program manager, was quoted in 1999, "If you really want to think far reaching, there's the possibility of a femtosatellite, essentially a solid-state satellite-on-a-chip, weighing 100 grams or less" [95]. This may be the first mention of *femtosatellite* in the literature. In 2006, CANEUS NPS announced, "The site for the world's first nanosatellite and satellite-on-a-chip manufacturing facility has been identified…and will be complete within six months" [96].

SSC is the first organisation to publish specific results on a monolithic implementation. *ChipSat* is an SoC research program aimed at miniaturisation of the small satellite platform. Initially, the objective of SSC research was to implement the on-board data handling sub-system of a small satellite on a single mixed-signal application specific integrated circuit (ASIC), which was to include enhanced remote sensing and data gathering payload capabilities [97]. The focus then shifted to a single-chip field programmable gate array (FPGA) implementation [98]. In addition, communication functionality was integrated into the single-chip on-board computer with sponsorship from ESA [98]-[102]. In 2003, SSC and SSTL presented their joint internal research and development portfolio suggesting that they were working "towards spacecraft-on-a-chip" [103]. From 2005 to 2008, incremental findings of this research are presented in [104]-[110] as the *SpaceChip* program, with final results discussed in Chapters 4 and 5.

2.3.2.3 Satellite-on-a-PCB

During the course of this research, the satellite-on-a-PCB or *PCBSat* approach originally served as a tangible prototype to guide the SpaceChip architecture development. Reviving a configuration similar to Stensat, shown in Figure 2-9 (right), but compliant with the P-POD deployer, PCBSat is the embodiment of the pursuit of the smallest useful satellite built out of COTS technologies and fabrication techniques. Interim results of PCBSat are published in [107], [111]-[113] with final results in Chapters 6 and 7.

2.4 Wireless Sensor Networks

The *wireless sensor network* concept emerged in the early 1990's, with academic roots that can be traced through an original group of researchers at the University of California, Los Angeles (UCLA) [114]. Various terms have been used to describe this concept over the past decade, yet *wireless sensor networks* has endured. In addition to developing the theory and supporting software, three hardware solutions for sensor nodes, sometimes called *motes*, were initially pursued: Smart Dust, COTS Dust, and Wireless Integrated Network Sensors (WINS).

Although the actual idea of Smart Dust is thought to have been born at a 1992 U.S. military workshop, Pister [115] is usually credited with coining the phrase and the first major development shortly after leaving UCLA for the University of California at Berkeley. The first Smart Dust implementation was a battery-powered MCM featuring a MEMS corner cube reflector for optical communications, as shown in Figure 2-15 (left) [116]. Pister's team went on to demonstrate a solar-powered variant soon after, shown on the right [117]. Much complementary work has gone into wireless communication protocols, with many leveraging COTS standards such as IEEE 802.11. New network protocols have been developed, including ad-hoc mesh networking. This research primarily focuses on the hardware development, also borrowing from these protocol developments.

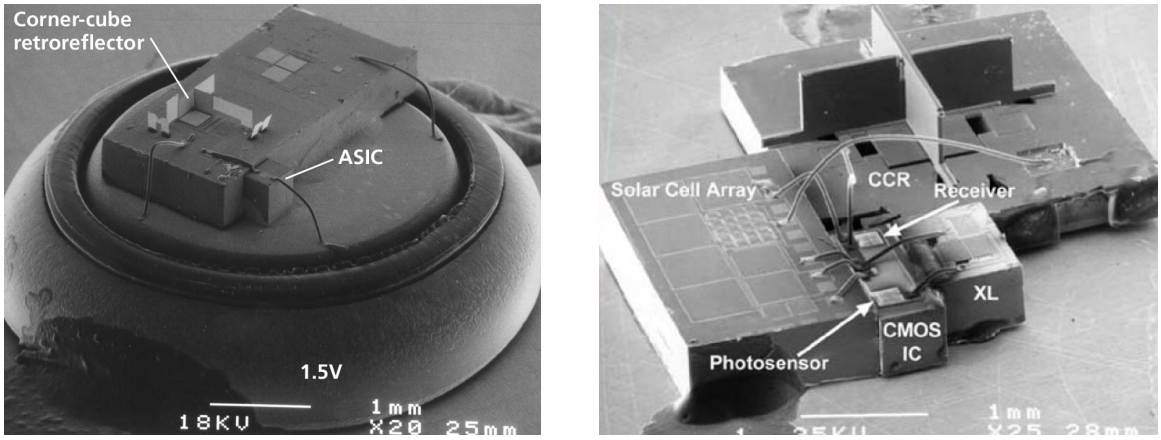

Figure 2-15. Battery Powered Smart Dust (left) [116] and Solar Powered (right) [117]

The new Berkeley team developed COTS Dust in parallel to Smart Dust. As shown in Figure 2-16, this concept was based on a PCB substrate with three versions utilising RF communications whilst one used optical [118]. Spin-off companies emerged, such as Crossbow, which now market the popular MICA family of motes. To simplify their implementation, the TinyOS operating system is now widely used in these systems.

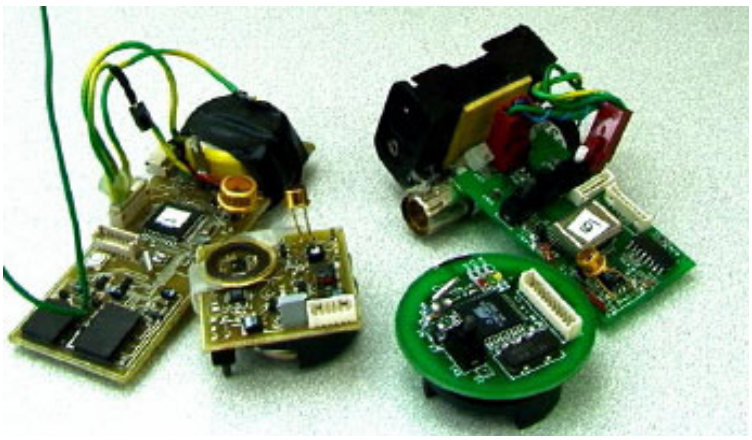

Figure 2-16. COTS Dust [118]

Whilst Smart Dust was in development, four of the original UCLA academics, led by Kaiser [119], pursued an RF-based SoC called WINS. Upon closer inspection, their approach was actually based on MCM integration of a sensor, microprocessor, and transceiver; which is similar to optical Smart Dust, but uses an RF link.

One of the most promising SoC projects is WiseNET, which has successfully integrated a radio, microprocessor, data storage, power control, and analogue interface, as shown in Figure 2-17 [120]. Although closer to a true SoC solution, the WiseNET sensor node still requires numerous external components, including a power source, passive devices, an antenna, and sensor.

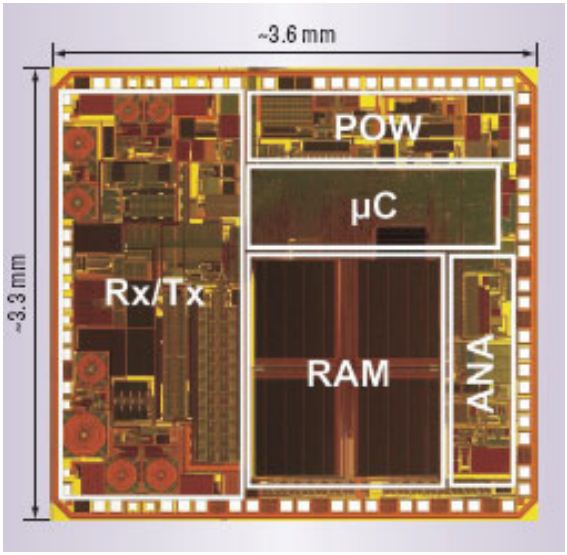

Figure 2-17. WiseNET Sensor Node [120]

In response to WiseNET, the Smart Dust team published a comprehensive investigation of an RF-based SoC approach [121]. It includes a discussion on the remaining work to realize a complete stand-alone SoC implementation. They concluded that although recent SoC solutions have demonstrated increased monolithic integration, many large off-chip components are still required, such as a sensor, battery, passives, crystal clock source, and RF antenna. Completed during the

same period, SSC's satellite-on-a-chip feasibility assessment, with similar objectives, arrived at the same conclusions [104].

Another technology related to wireless sensor networks is Radio Frequency Identification (RFID). The basic concept was explained in 1948 and arguably was envisaged before this time [122]. This technology was not used much until the 1970s, when it saw some widespread use in automated vehicle identification for various purposes, such as toll roads. Technology has allowed miniaturisation to the point where RFID "tags" can be made monolithically, including an antenna, with a range of a few metres, passively powered by the interrogating RF signal [123].

2.5 Summary

This chapter presents the state-of-the-art with a problem-solution structure. The challenge is that numerous envisaged distributed space missions with high payoffs are awaiting technical solutions. Most of the academic excitement currently surrounds a few missions that require small clusters of formation flying satellites, which is a complex proposition. In contrast, there is an undeniable trend toward massively distributed space missions to enable science missions requiring multipoint remote sensing or in-situ observations. These architectures require hundreds to thousands of low cost, mass producible satellites. For example, this concept could demystify ionospheric plasma depletions, thought to cause problematic satellite signal outages.

Spacecraft miniaturisation is the ubiquitous theme of the satellite industry. Very small satellite technologies have been examined in the context of supporting the space sensor network concept. Microengineered aerospace systems and traditional picosatellites offer possible solutions, but may not be the most cost effective as they rely on new or labour-intensive fabrication techniques. Emerging technologies revived in this research, satellite-on-a-chip and satellite-on-a-PCB, are discussed in detail in Chapters 4 through 7. All technologies discussed can leverage the hardware and communication protocols developed by the now prolific wireless sensor networks. A common mission framework is proposed in Chapter 3, by which all technologies discussed in this research can be compared by cost and performance, reported on in Chapter 8.

Chapter 3

3 Space Sensor Network Architecture Design

This chapter applies a generalized approach to space sensor network design. Section 3.1 expands on the discussion given in Section 2.2.2.4 regarding a family of space weather missions that could be greatly enhanced by a space sensor network. A case study mission is selected in Section 3.2, targeting problematic ionospheric disturbances that are thought to cause communication and navigation satellite signal disruption. The majority of the chapter, Section 3.3, is devoted to a detailed discussion of the mission design and development of specific requirements.

3.1 Introduction

A selection of space weather induced anomalies is presented in [112] and reviewed in this section, focusing on the ionosphere, which is an ionized and dynamic component of the upper atmosphere. The ionosphere begins at approximately 80 km in altitude and slowly disperses through LEO. Not only does this directly present a unique space environment for satellites in LEO, but can also affect RF communications between ground users and satellites in any orbit. Understanding and predicting space weather and specifically the mechanisms of the ionosphere has become an urgent requirement as our society continues to grow more dependent on space-based assets.

Like any communications medium, variations in the ionosphere can deflect or alter RF signals passing through. These phenomena can be as small as a few centimetres up to thousands of kilometres and have been studied since the 1930s using in-situ and remote sensing measurements. However, small-scale variations (metres to kilometres) have only recently come under closer study [124]. Small-scale variations in ionospheric density have been observed by in-situ spacecraft passing periodically through regions of interest, and by remote techniques, which effectively integrate observed variables over small regions in space and time.

A constellation of sensor nodes can make multiple in-situ point source measurements of ionospheric density and temperature over scale sizes from centimetres upwards. Such missions have been proposed, but have unfortunately never materialized [34]. Intersatellite spacing on the order of 10 cm requires a data-sampling rate of 10 μs or faster to resolve space-time ambiguities in LEO, so larger spacing is preferred to minimise the system requirements. Three potential missions from [112] utilising a constellation of sensor nodes are briefly discussed.

The *dayside mid-latitude trough* is a persistent feature of the post-noon winter auroral ionosphere, located 10-20 degrees equatorward of the nominal auroral oval [125]. The equatorward trough wall is dominated by solar ionisation extending from daytime through twilight, whereas the poleward wall may be caused by particle precipitation. Flux tubes complicate this phenomenon. Current ground-based observations using radio tomography, coherent, and incoherent scatter radar have a resolution of tens of kilometres [112].

A distributed mission flying through the mid-latitude trough region (~50 degrees inclination, ~350-600 km altitude), utilising ion density and temperature sensors and dual-phase radio transceivers, would enable both high resolution point source and radio tomographic mapping of the ionospheric volume within the constellation. Satellite separations would need to be hundreds of metres to tens of kilometres, using tomography to complement and extend the resolution and range of ground-based measurements. Individual ion sensors will need to take data at a sub-millisecond cadence, generating a significant amount of data. This would complement the comparatively low resolution, broad coverage ionospheric mapping currently available from satellite-to-ground tomography/radar techniques, and sparse ionosonde data [112].

The dominant production mechanism of large-scale travelling atmospheric disturbances or gravity waves is thought to be *Joule heating of the neutral atmosphere* [126]. Whilst some sources of Joule heating can be studied from ground-based sensors, the small-scale electric field variability component requires in-situ measurements using neutral/ion spectrometers and magnetometers at meter to kilometre scales over several hours [112].

Small separations between spacecraft (centimetres to hundreds of metres) are highly desirable in order to characterize the atmosphere on these scale sizes. Very high cadence data taking will be required, whilst on-board data analysis and compression would mitigate the high volume data download requirements. Direct measurements of ion and neutral fluxes require attitude determination to a high precision (of the order of degrees), with at least one axis (preferably three) stability and multiple instruments [112].

Ionospheric plasma depletions, otherwise known as *plasma bubbles*, [33] typically occurring in LEO at low latitudes after local sunset, are gravitationally driven instabilities peculiar to the equatorial ionosphere. Once formed, the bubbles propagate at speeds of tens or hundreds of metres per second and can rise rapidly through buoyant convection where they may deplete entire magnetic flux tubes. A mid-latitude orbit (~30-35 degrees inclination, ~350-500 km altitude) would be required with sensor separations of metres to hundreds of kilometres measuring plasma density and temperature. This mission is selected for a case study application of a space sensor network based on very small satellites [112].

3.2 Case Study Mission: Plasma Bubbles

Plasma bubbles are believed to cause communication and navigation satellite signal outages by *scintillating* the signal as conceptually illustrated in Figure 3-1. Testimonials of disruptions to commercial, government, and military operations have made forecasting scintillation a top priority. The $100 million (estimated) single-satellite Communication and Navigation Outage Forecasting System (C/NOFS), launched on 17 April 2008, is the first satellite mission solely dedicated to studying and forecasting plasma bubbles. Its mission requirement is to forecast equatorial plasma instability for the next two to six hours in addition to a three-day outlook. C/NOFS's elliptical orbit is 400x700 km with a 13 degree inclination [127]. The U.S. Defense Meteorological Satellite Program (DMSP) satellites make similar measurements over polar orbits. Datasets from the C/NOFS and DMSP satellites, together with ground-based detectors integrating over volumes of space, will be assimilated into global predictive models.

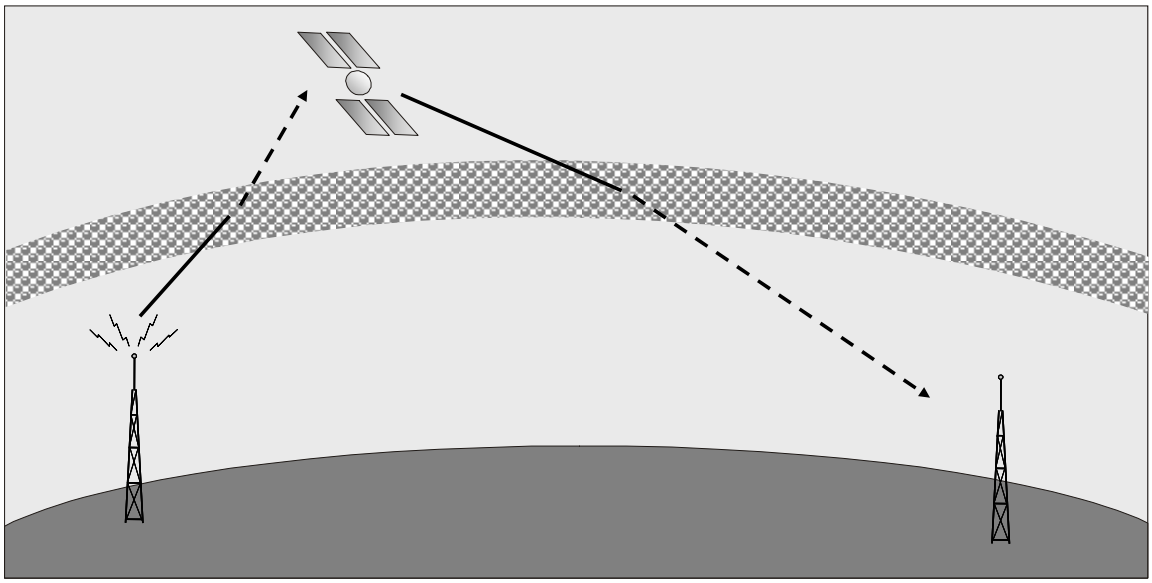

Figure 3-1. Plasma Bubble Induced Signal Scintillation

A mission consisting of a sensor network constellation in LEO measuring the plasma density and temperature at specific time/location intervals would provide additional data points to the C/NOFS dataset, helping to quantify the accuracy of the forecast model. Physical separations of the sensors would partially resolve some of the space/time ambiguities, which are inherent in taking point-source measurements with a single spacecraft [112].

The measurement of plasma parameters, and inferences made about spatial and temporal structuring in the local volume envelope, will aid in validating and improving physical models of plasma bubble formation and propagation. It will also contribute more known truth measurements to assimilative models. The goal is to produce models able to forecast scintillation through plasma bubble indicator proxies [112].

3.3 Space Mission Analysis and Design Process

The Space Mission Analysis and Design (SMAD) process is outlined in Table 3-1, adopted from Table 1-1 in [11]. The SMAD process is a guide, which can be specifically adapted to a particular organisation. NASA, ESA, and other governmental agencies have developed their own acquisition processes based on lessons learned and particular organisational needs. The SMAD process guides the organisation of this section.

Table 3-1. Space Mission Analysis and Design Process [11]

▪ Define Objectives	1. Define broad objectives and constraints
	2. Estimate quantitative mission needs and requirements
▪ Characterize the Mission	3a. Define alternative mission concepts
	3b. Define alternative mission architectures
	3c. Identify system drivers for each
	4. Characterize mission concepts and architectures
▪ Evaluate the mission	5a. Identify critical requirements
	5b. Evaluate mission utility
	5c. Define mission concept
▪ Define Requirements	5d. Define system requirements
	5e. Allocate requirements to system elements

3.3.1 Broad Objectives and Constraints Definition

Most space missions set out to address a specific problem. This is also true in this research; however, the primary objective in this case is to demonstrate the utility of a space sensor network architecture enabled by very small satellites. In order to exhibit its value, a fundamental user-driven problem has been targeted to augment ongoing research. The plasma bubble mission statement and objectives are given in Table 3-2. The overarching constraint is to use COTS components, fabrication techniques, systems, launch vehicles, and deployers to keep costs low.

Table 3-2. Plasma Bubble Mission Statement and Objectives

▪ Mission Statement	Ionospheric plasma depletions, otherwise known as plasma bubbles, are thought to be a primary source of satellite communication and navigation signal outages experienced by ground users, mostly in equatorial regions. Current sparse ground and space-based sensor systems that study this phenomenon are not adequate to model and predict plasma bubble occurrence. A space sensor network providing multi-point in-situ measurements of the phenomenon is required.
▪ Primary Objective	To demonstrate the utility of a space sensor network based on very small satellites as a low-cost approach to solve a fundamental user-driven mission
▪ Secondary Objective	To detect and measure plasma density and temperature at various points of the ionosphere simultaneously

3.3.2 Quantitative Mission Needs and Requirements Estimation

Currently, there is a three-order of magnitude (1000:1) disparity between ground and space-based weather sensors. The number of space and terrestrial sensors focused on space weather is shown in Figure 3-2 [128]. Similarly, the number of fixed terrestrial sensors is shown in Figure 3-3 [129], whilst the daily coverage from space-based assets is shown in Figure 3-4.

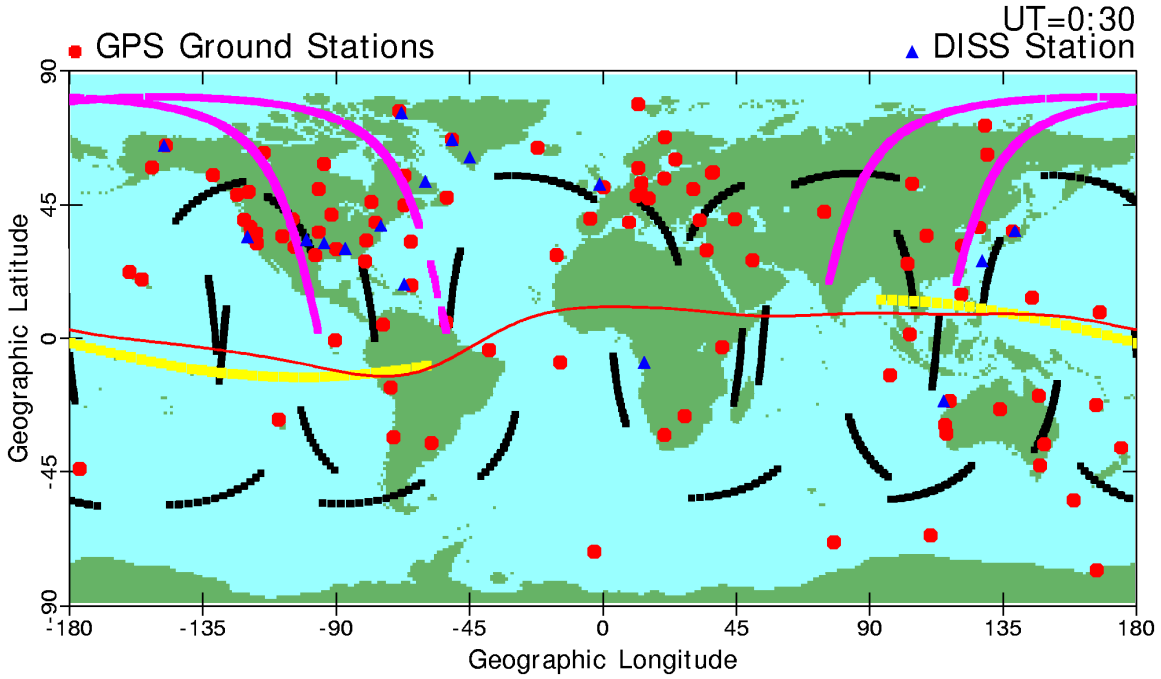

Figure 3-2. Space-Focused Weather Sensors [128]

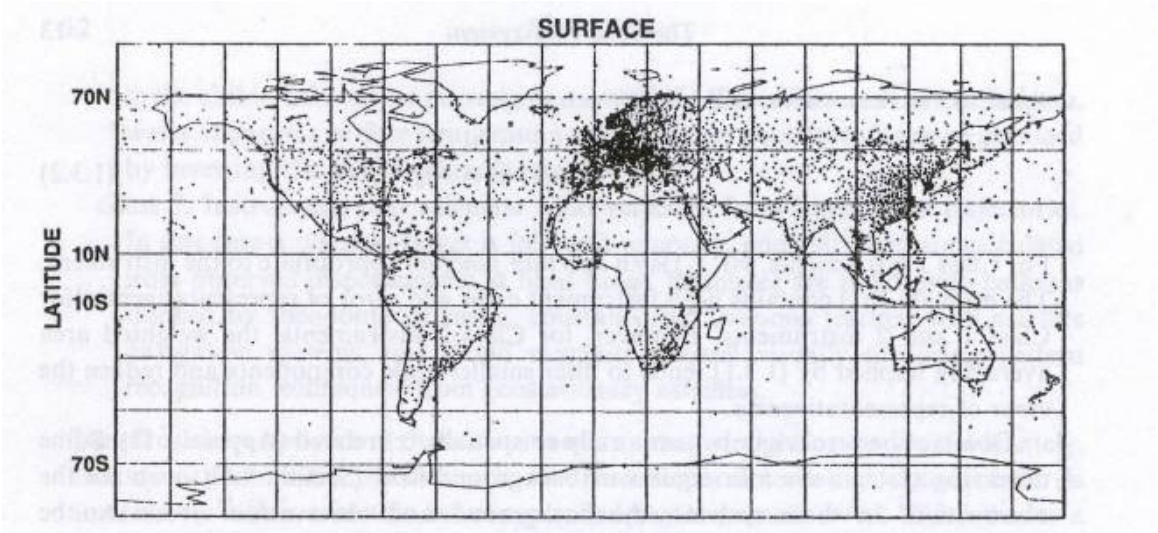

Figure 3-3. Fixed Terrestrial Weather Sensors [129]

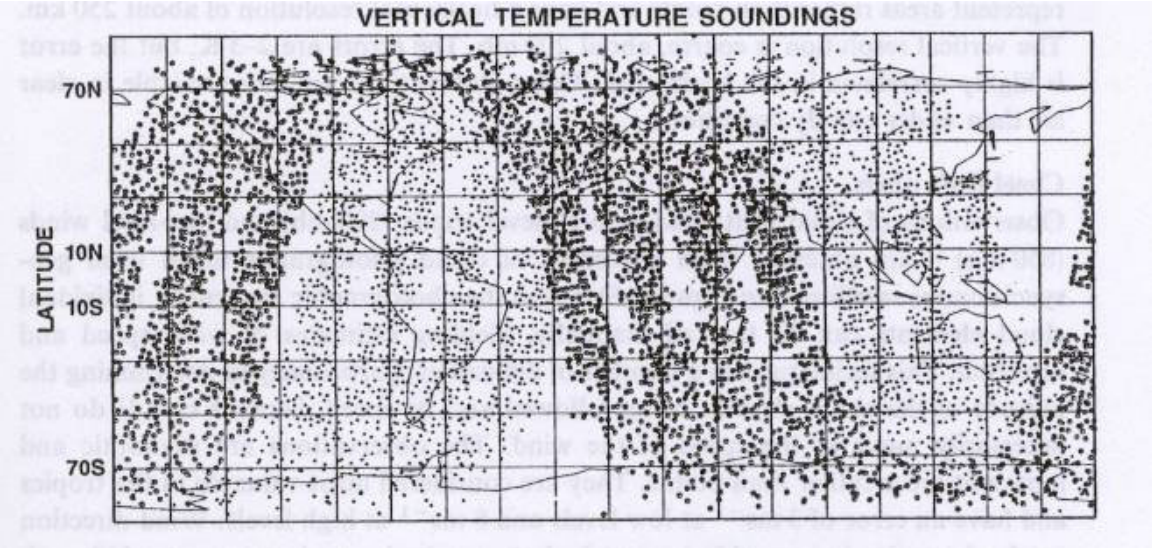

Figure 3-4. Daily Coverage of Space-Based Terrestrial Weather Sensors [129]

With only a dozen or so space-based sensors in existence, any mission that could even double the amount of sensors in a single deployment would be of significant scientific value. In other words, space weather is conclusively under sampled. Terrestrial weather forecasting requires sampling of the relatively neutral temperature, pressure, and winds. Similarly, space weather forecasting requires sampling of the plasma temperature and density, along with neutral winds.

For the case study mission, a few simple quantifiable objectives are proposed. Distributed simultaneous in-situ measurements are required of the plasma density and temperature once per second. Distributions of a few metres to tens of kilometres would return sufficient data to judge the utility of the mission. Mission objectives and constraints are summarized in Table 3-3.

Table 3-3. Plasma Bubble Quantified Mission Objectives and Constraints

▪ Measurements	Plasma density and temperature
▪ Frequency	1 Hz
▪ Measurement points/satellites	As many as practical
▪ Distribution	1 m – 100 km
▪ Mission cost	Less than $500,000
▪ System components and deployer	COTS

3.3.3 Alternative Mission Concepts and System Drivers

Typically, when a new space mission is proposed, a careful examination is made of potential alternative mission concepts. For example, the FireSat case study discussed in [11] trades off terrestrial versus space-based sensors. Where space-based missions are required, such as in-situ measurements as in the case of plasma bubbles, the space sensor network is the proposed alternative mission concept versus the existing sparse monolithic satellites. The cost and performance drivers of all very small satellite technologies discussed throughout this research are

presented in Chapter 8. The common system drivers are listed in Table 3-4 along with the approach for this mission based on Table 2-8 in [11].

Table 3-4. Common System Drivers and Approach

▪ Size	As small as possible
▪ Mass	As low as possible
▪ Power	Tradeoff between size, cost, duty cycle
▪ Data rate	Minimum to meet the objectives
▪ Communications	Intersatellite and ground links
▪ Pointing	Determined by payload
▪ Number of satellites	Minimum to determine mission utility
▪ Altitude	Appropriate for plasma bubble study and debris mitigation
▪ Coverage	Appropriate for plasma bubble study
▪ Operations	Store and forward, supported by autonomous ground station

3.3.4 Mission Concept and Architecture Characterisation

Mission concept and architecture characterisation consumes most of the effort in mission design as it clearly defines the system makeup and function. Beginning with the quantified mission objectives and constraints summarized in Table 3-3, the mission is characterized using the process flow outlined in Table 3-5 along with the factors that must be considered. The organisation of this Section 3.3.4 follows this flow.

Table 3-5. Mission Concept and Architecture Characterisation

1.	Preliminary mission concept	Documentation and mission timeline
2.	Subject characteristics	Active/passive, spectral coverage, duty cycle
3.	Orbit and constellation	Temporal and spatial coverage, number of satellites
4.	Payload	Performance, size, mass, power, pointing, stationkeeping
5.	Mission operations approach	Orbit determination, command, control, communications
6.	Spacecraft bus	Size, mass, power pointing, propulsion, performance
7.	Launch and deployment	Launch vehicle, deployment, orbit transfer
8.	Mission logistics	Mission execution and end-of-life

3.3.4.1 Preliminary Mission Concept

The preliminary mission concept is to deploy multiple very small satellites linked wirelessly to take distributed, in-situ measurements of ionospheric plasma depletions. The constellation will not be maintained, but rather allowed to disperse naturally based on orbital perturbations. Any demonstration of this nature will return valuable results, so setting low objectives is paramount to ensure first mission success. Real-time or high-tempo tasking and scheduling will not be attempted. Instead, single-orbit measurement campaigns will be selected, executed, processed, and analyzed from a single ground station running autonomously. A depiction of the mission is shown in Figure 3-5, illustrating both the wireless network and natural dispersion concepts.

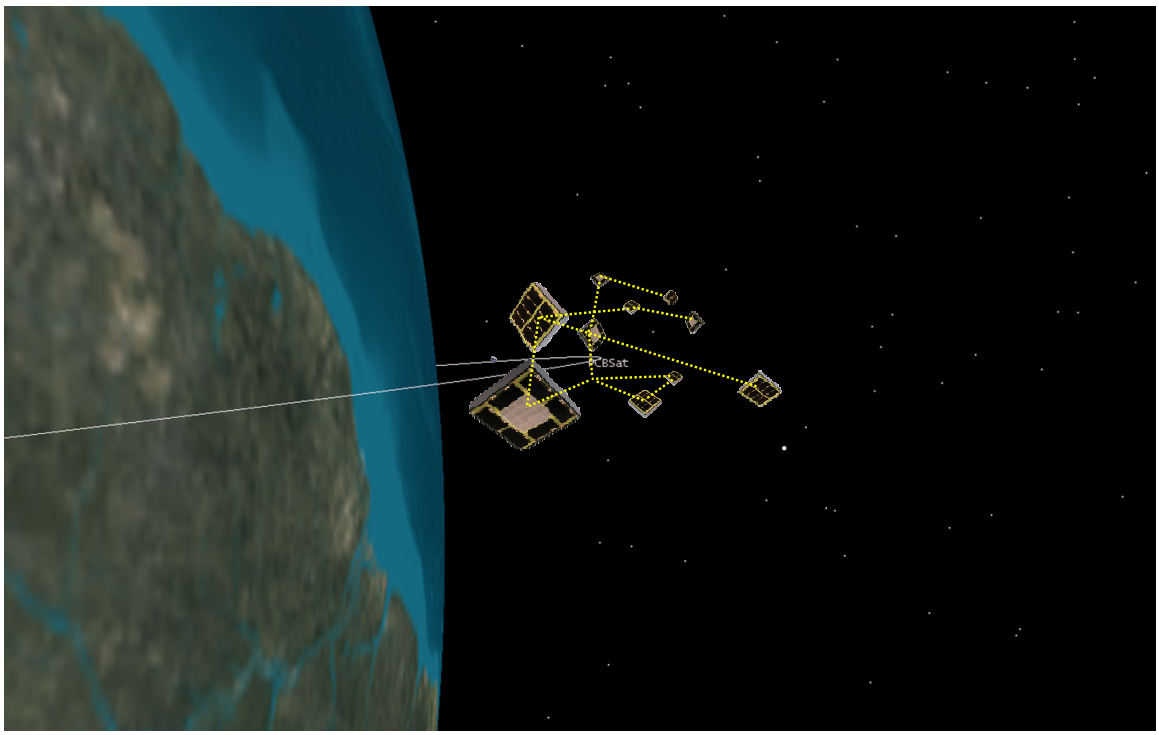

Figure 3-5. Depiction of Preliminary Mission Concept

3.3.4.2 Subject Characteristics

The subject of the mission is *ionospheric plasma depletions* or *plasma bubbles*, which is a phenomenon that largely occurs at near-equatorial latitudes in the ionosphere for several hours after local sunset as depicted in Figure 3-1 and fully described in [33]. For simplicity, plasma bubbles can be thought of as being similar to bubbles in a swimming pool or lava lamp, although they can move in any dimension.

3.3.4.3 Orbit and Constellation

A variety of LEO options are suitable (~10–100 degrees inclination, ~300–500 km altitude) provided it allows sensors to enter and exit the region of interest (+/- 10 degrees latitude below 700 km) to establish baseline and disturbed measurements. Orbit control is not required or desired, as the natural perturbations will serve to alter the distribution and lower the altitude over time without adding the complexity of a propulsion subsystem. This will allow variations in the measurements and will address orbital debris concerns of space sensor networks, as the mission will be sufficiently short lived. Characterising this natural drift has proved to be difficult, as this specific implementation is sparsely discussed in the literature due to the novelty of the concept.

This section is not intended to be a treatise on the subject, but rather a conceptual discussion. Simulation tools, such as Satellite Tool Kit (STK), even with its high-precision orbital propagator, are of questionable value in modelling this case, as they are only as valid as the input data

provided and the atmospheric models. Regarding a constellation of multiple very small satellites, one must step through the deployment scenario in order to investigate the sources of orbital perturbations and examine their potential effects.

Using a COTS deployment system, as discussed in Section 3.3.4.7, a batch of three to twelve very small satellites can be ejected from one deployer. Although multiple deployers can be manifested on the same launch vehicle, this initial mission focuses on a single deployment. Typically, the satellites are deployed at a relative velocity of 1.5 to 2 m/s by a large spring mechanism [130]. Furthermore, two separation springs are placed between each satellite to guarantee displacement of all satellites to avoid potential re-contact [131]. A separation velocity of at least 188 mm/s can be expected, as estimated by Equations 3.1 and 3.2, assuming a 1 kg satellite mass, dual 6.7 N force springs, and a 1.32 mm travel distance. At this rate, the satellites will drift apart approximately 10 km/day. This dramatically shortens the mission lifetime, as even metre-scale intersatellite measurements are useful, in addition to quickly exceeding the communication range.

$$F = ma \tag{3.1}$$

$$v^2 = v_0^2 + 2a(x - x_0) \tag{3.2}$$

An unorthodox approach is suggested for the deployment of a space sensor network using very small satellites. Using the same deployment system, a batch of satellites could be "bailed" using monofilament line, typically used for fishing. Monofilament line is particularly susceptible to degradation when exposed to UV radiation. With this approach, the batch of satellites would deploy together as depicted in Figure 3-6 (Phase 1). Within a few days, the UV radiation combined with a near vacuum will cause the line to become brittle, eventually breaking, allowing the satellites to gently separate (Phase 2). Monofilament line has often been used by the amateur and academic satellite communities for deployment of measuring tape style antennas [132]. Similarly, deployable antennas, restrained by thicker monofilament line, will deploy shortly after (Phase 3). This will provide a slight disturbance to separate the spacecraft in addition to the force of an intentionally weak separation switch spring. Additionally, the antennas will serve to passively control the attitude depending on payload requirements (Phase 4). The hardware implementation is fully described in Chapters 6 and 7, with attitude control in Section 6.7.

Once the satellites separate, the mission begins. At this point, one must consider the natural orbital perturbations, both short and long-period variations, to determine at what rate and relative direction the satellites will separate from one another. The drag environment in LEO is the largest orbital perturbation to consider, which causes the orbits to lose energy, eventually resulting in re-entry. Solar radiation pressure must also be considered for satellites with low ballistic coefficients

[133]. Some argue that intersatellite Coulomb forces should be considered when separation distances are less than ten metres, which will be the case early in this scenario [134]. Third-body and nonspherical Earth perturbations will not be considered, as these forces are assumed to act equally on all satellites in the constellation, but may become a factor as they spread significantly.

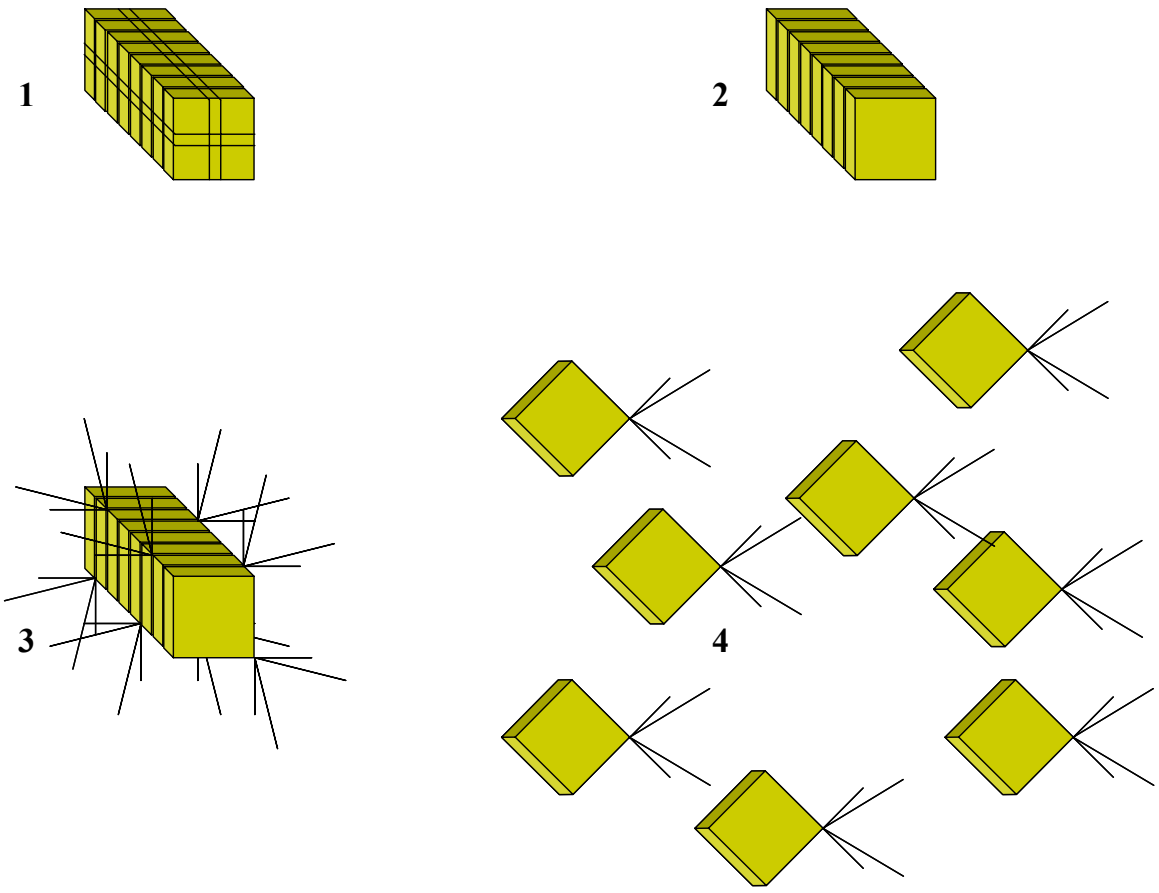

Figure 3-6. Depiction of Deployment Concept

Considering the drag force first, one must understand the components of the force as given in Equation 3.3. Here, F_d is the drag force (acting along the velocity vector), m is the satellite mass, a is the resulting deceleration, ρ is the atmospheric density, C_d is the drag coefficient, A is the projected area of the satellite normal to the velocity vector, and v is the satellite velocity, as given by Equation 3.4, for a circular orbit. The orbital velocity is a function of the Earth gravitational parameter, $\mu_\oplus$ and the orbit altitude, h.

$$F_d = ma = \frac{1}{2}\rho C_d A v^2 \tag{3.3}$$

$$v = \sqrt{\frac{\mu_\oplus}{h + R_\oplus}} \tag{3.4}$$

Assuming for a time that the satellites are in close proximity and that each satellite is identically constructed, all of the variables in Equation 3.3 for each satellite should be identical during this initial period. Since the goal is to spread the satellites out with a low relative velocity, one or more of the variables must differ between satellites. One source of random variation could be the arrangement of the deployable antennae, which would affect the projected area *A*. Setting a maximum variation of 1% in *A*, a notional simulation in STK, given the input parameters shown in Table 3-6, illustrates the satellite dispersion 24 hours after separation as shown in Figure 3-7. The viewpoint is 300 metres from PCBSat0 and the satellite spacing is only 6 metres.

Table 3-6. Satellite Tool Kit Simulation Parameters

▪ STK version	8.1.0
▪ Propagator	High Precision Orbital Propagator (HPOP)
▪ Number of satellites	10
▪ Orbit	500 km circular, 30 degree inclination
▪ Start date	1 July 2011 (near solar maximum)
▪ Frontal projected area, *A*	35.355 cm^2 (.0035355 m^2)
▪ Satellite mass	300 grams
▪ Drag Area/mass ratio	0.011785 m^2/kg
▪ Variation in *A*	1% in 0.1% increments among all satellites
▪ Drag coefficient	2.2
▪ Area exposed to sun	100 cm^2
▪ Solar radiation pressure reflectance	1
▪ Atmospheric density model	Jacchia-Roberts
▪ All other options	Default

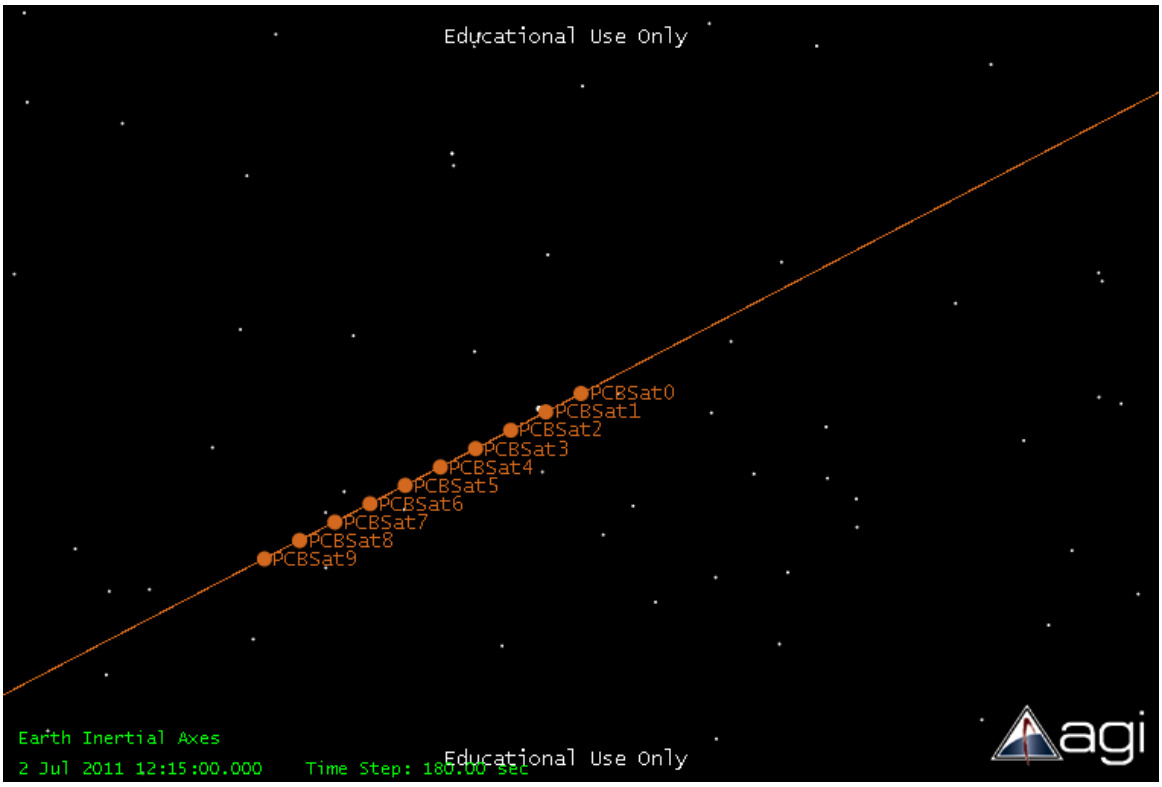

Figure 3-7. Satellite Separation of 6 m Considering Drag Only after 24 h (300 m view)

As shown in Figure 3-7, the atmospheric drag only produces a separation within the plane of the orbit, i.e. a two-dimensional configuration. To make three-dimensional measurements, out of plane variations are required, such as altering other orbital elements besides the semi-major axis. To accomplish this, solar radiation pressure can be leveraged, which is proposed and fully described for picosatellites in [133]. Solar radiation pressure is calculated with Equation 3.5, where r is the reflection factor and A is the area exposed to the sun. By simply varying the reflection factor by applying random amounts of reflective tapes to inactive surfaces of the satellites (not over solar arrays), small three-dimensional variations can be realized. Results from a second STK simulation, where the reflection factor is incrementally varied from 0.8 to 0.9 between the spacecraft, is shown in Figure 3-8. All other parameters are the same as in Table 3-6.

$$F_{srp} = ma = -4.5 \times 10^{-6}(1+r)A/m \tag{3.5}$$

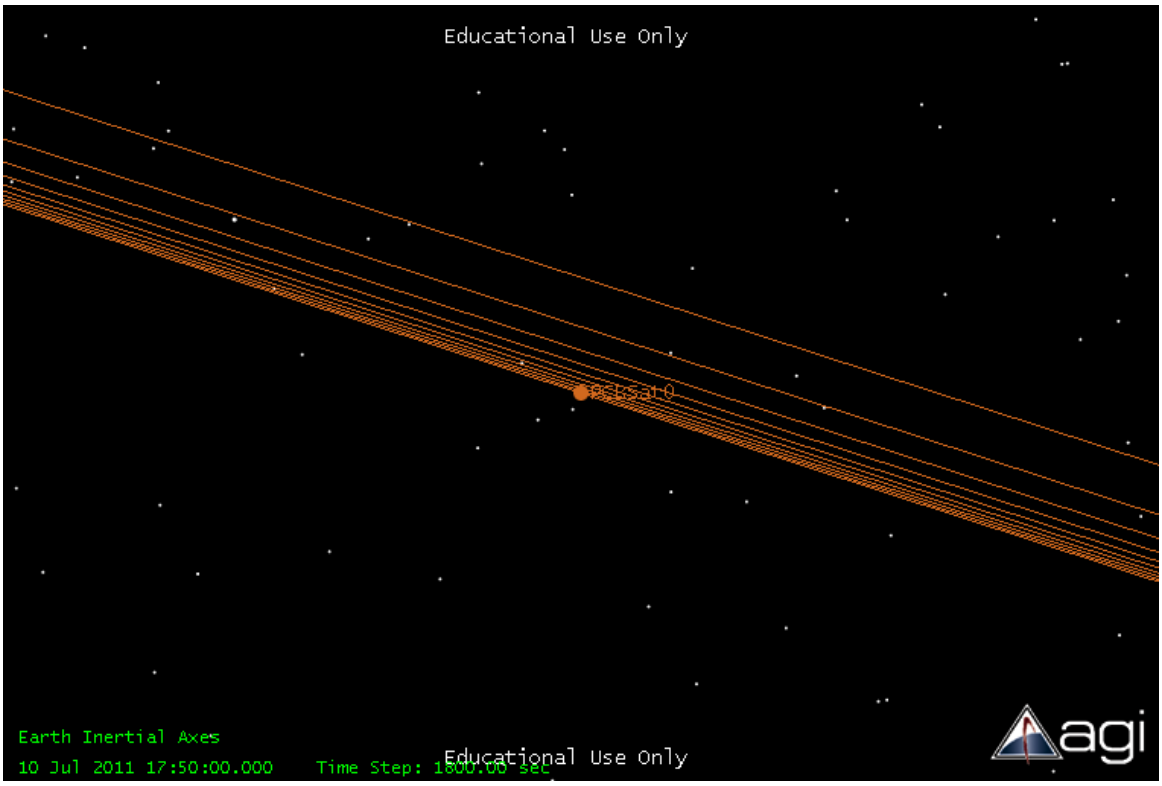

Figure 3-8. Satellite Separation Including Solar Radiation Pressure after 10 d (300 m view)

Regarding the orbit and constellation design, one must also consider the communication range among satellites and from the satellite to the ground. This is discussed in more detail in Section 3.3.4.5, but must be mentioned in the context of constellation design. Miniature intersatellite radios are available with a maximum range of approximately 100 km. A longer-running STK simulation with the same basic parameters as before reveals that the intersatellite spacing exceeds 100 km in approximately four months as shown in Figure 3-9.

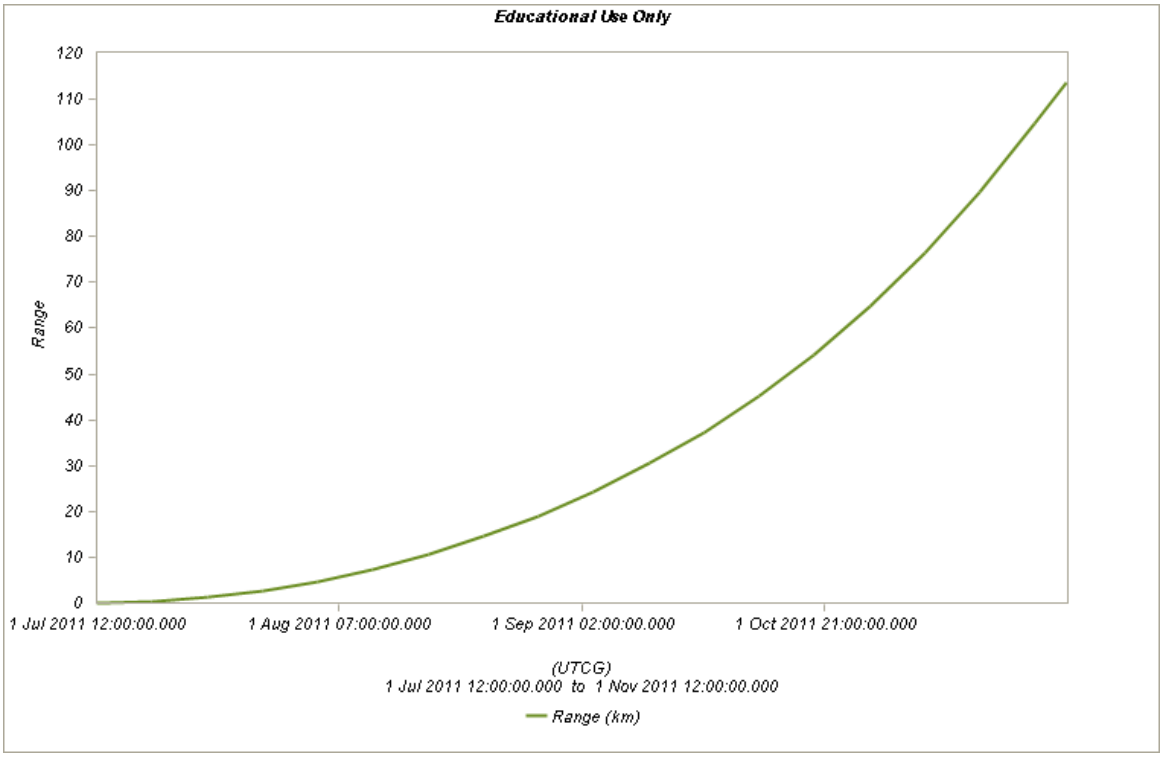

Figure 3-9. Satellite Separation Including Solar Radiation Pressure at Four Months

Very small satellites have limited power and volume within, which may constrain the ability for a direct ground link. This is further discussed in Section 3.3.4.5, but must also be considered, as it is conceivable that a relay satellite with a stronger downlink may be required. CubeSats, as discussed in Section 2.3.1.2, have frequently demonstrated successful uplinks and downlinks, but have yet to demonstrate a crosslink within a constellation. Using a CubeSat as a relay satellite within a constellation of very small satellites presents an additional challenge in assuring a long duration of close proximity, as the mass and shape of the spacecraft are different. However, *ballistic coefficient matching* of all satellites in the constellation can be used to reduce the separation rates. Revisiting Equation 3.3, the ballistic coefficient (BC) is typically expressed as in Equation 3.6. The *m/A* ratio can be easily matched, when the frequently assumed value of 2.2 is used for the drag coefficient. Through matching, the dispersion is nearly identical to the simulation results just presented. However, dissimilar shapes undoubtedly will produce different drag coefficients. Unfortunately, exact determination of C_d is only possible through on-orbit investigations, as it varies by altitude and other factors [135]-[136]. A detailed investigation of this aspect is beyond the scope of this research, therefore identical drag coefficients are assumed for a similar orientation and deployed antenna characteristics.

$$BC = \frac{m}{C_d A} \tag{3.6}$$

3.3.4.4 Miniaturized Electrostatic Analyzer Payload

Traditionally, cost and launch vehicle capacity are constraints in determining the maximum spacecraft size. Miniaturized satellite payload sensors become the chief system driver regarding small satellites, as the aim in this research is to derive the smallest satellite possible. Compact, low-power ionizing devices are being developed that would ionize the neutral gas entering the device after ambient ions have been rejected [137]. This miniature sensor could be used to study the Joule heating sources mission discussed in Section 3.1.

The Miniaturized ElectroStatic Analyzer (MESA) has been developed to provide a low-cost, low-impact sensor to record ion and electron densities and temperatures around LEO satellites [138]. The sensor can be used in other orbits as well, provided the supporting electronics can tolerate the radiation environment and address any spacecraft charging issues. MESA was originally developed for flight on the U.S. Air Force Academy's FalconSAT-2 as a low-cost low-impact "peel and stick" sensor capable of being integrated onto any three-axis stabilized satellite [139]. Following the failure of the first SpaceX Falcon-1 launch vehicle carrying FalconSAT-2, MESA was integrated into the MISSE-6 mission on the International Space Station (ISS) and has been selected as a payload on four other LEO satellite missions (FalconSAT-5, PnPSAT, AndeSAT, and MISSE-7) [112].

The basic sensor plates are shown alongside a self-contained version on the left and right sides of Figure 3-10. The sensor plate stack alone measures 60×60×5 mm and 80 g for this particular implementation. Although the thickness of the stack is fixed, the other dimensions can be varied as required. A stand-alone, encapsulated configuration with supporting electronics has been developed for the MISSE-6 experiment package. It has a mass of 150 grams, requires 300 mW of power, and produces data at a rate of 6 kB/sec in high-resolution mode.

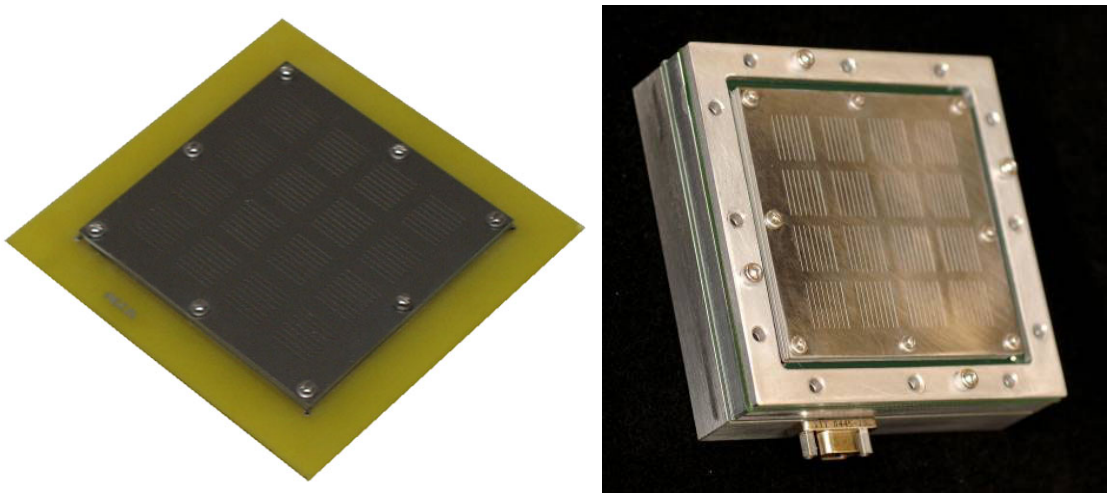

Figure 3-10. MESA Sensor Plate Stack (left) and Encapsulated (right) [138]

The instrument is an ion or electron spectrometer, where charged particles are steered through an 'S-bend' by an electric field between two plates, biased with the same polarity as the species of interest. The energy passband is selected by the geometry of the plates, the applied voltage across them, and the separation and size of the entrance and exit collimating apertures. A schematic of the instrument is shown in Figure 3-11, illustrating a SIMION (ion simulation software tool) trace of ions entering the spectrometer on the left, passing through a first collimation stage, then being deflected by an electric field between the upper and lower central bias plates. The ions exit through a second collimation stage and impinge on a current collector plate, which is essentially a large PCB copper pad [112].

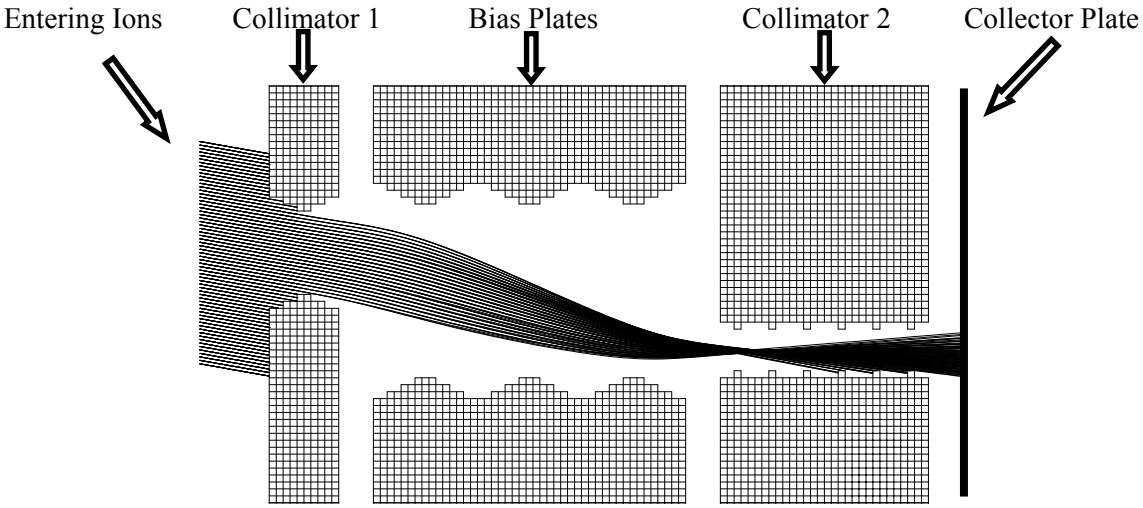

Figure 3-11. Cutaway of the MESA Sensor [112]

Sweeping the applied voltage allows particles of differing energies to be steered through and spectra to be taken, producing a curve with assumed Maxwellian distribution where the density is the peak of the curve and the width is the temperature. A positive bias on the collector plate indicates the presence of ions whilst a negative bias indicates electrons. Optional on-board processing allows multiple collection modes, pre-processing, and selective compression of data. Combined with on-board storage, this allows intelligent data collection when real-time high-speed telemetry is unavailable. Diagnostic modes allow for full spectra over the energy range 0-20 eV with step sizes as low as 0.01 eV to be produced at a consequently higher data-producing rate.

The basic MESA data packet requirements are shown in Table 3-7. The raw diagnostic data does not need to be stored or transmitted once the validity of the on-board estimation is established. During normal operations, each spacecraft will produce 448 bps (56 Bps from Table 3-7) during a typical 35 minute (2100 s) LEO eclipse for a total of 941 kb/eclipse (448 bps × 2100 s). The data is stored internally during the eclipse then forwarded through the wireless network in the sun as time and resources permit. Assuming a demonstration mission of ten very small satellites, this results in 9,410 kb/eclipse that would be forwarded to the relay satellite.

Table 3-7. MESA Data Packet

Bytes	Description
3	Unique identifier and status flags
17	Time and location stamp
250	MESA raw data (optional)
36	Processed MESA data
306	**Total (diagnostic)**
56	**Total (normal)**

Measuring ions (typically oxygen or hydrogen) requires that the MESA face be oriented in the ram direction to within +/- 4 degrees in pitch. Thus, MESA can be used to assist in confirming orientation prior to establishment of three-axis stability in a larger satellite with attitude control. Electrons in LEO can be measured with the sensor at any attitude, and the electron density can be used to estimate the ion density (or vice versa) by assuming quasi-neutrality of the plasma. The only other major constraint is that the local magnetic field must be kept less than 0.2 Gauss.

3.3.4.5 Mission Operations Approach

The goal for mission operations is to be as simple and low cost as possible. A single OSCAR (Orbiting Satellite Carrying Amateur Radio) class groundstation using ultra-high frequency (UHF) and very high frequency (VHF) bands with automated antenna tracking will comprise the ground segment. Numerous CubeSats missions have reliably demonstrated 9,600 bps downlinks or better with amateur ground stations and publically available orbital element updates from space object tracking organisations. A typical ten minute pass will allow the download of 5,760 kb, which is more than adequate, if two consecutive passes are used for download with no measurement campaign in between. COTS VHF/UHF communications modules are now available for CubeSats [140].

There is interest in using 2.4 GHz Instrumentation, Scientific, and Medical (ISM) band COTS radios for a higher speed downlink, up to 115.2 kbps. The ISM band is license free, which is a major consideration, as obtaining a frequency license can be one of the most difficult aspects of developing a new mission [141]. The NASA GeneSat-1 mission, using a triple CubeSat form factor, demonstrated the use of the Microhard MHX-2400 2.4 GHz ISM radio [142]. Due to the higher data rate and frequency, the one watt RF transmitter could only be heard 33% of the time, even with the use of an 18-m groundstation dish. However, 100% of the data was transmitted and received using receipt acknowledgement protocols. Although this type of radio does not seem well suited as a downlink, it is ideal for intersatellite links in a space sensor network. Many COTS radios now include ad-hoc mesh networking protocols. These issues are discussed in more detail in Section 6.6.

3.3.4.6 Spacecraft Bus Design and Space Environment Issues

The purpose of the spacecraft bus is to support the payload in accomplishing the mission. In the very small satellite domain, traditional picosatellites and microengineered aerospace systems options are reviewed in Section 2.3. Two revived options; satellite-on-a-chip and satellite-on-a-PCB, are presented in Chapters 4 through 7, respectively, where all subsystems are discussed and applicable detailed designs presented. All technologies are compared in Chapter 8.

System-level space environment issues must be considered for all technologies as presented in Table 3-8. This environment complicates system design.

Table 3-8. Space Environment Considerations

▪ Mechanical	shock, vibration, acceleration
▪ Atmospheric	corrosion, debris, vacuum
▪ Thermal	extremes, limited heat transfer
▪ Energetic	radiation, including charged particles
▪ Dynamic	free-fall orbit, high velocity mobility, attitude disturbance torques

In general, mechanical hazards are an issue for the system level. Most terrestrial components can withstand the shock, vibration, and acceleration encountered during the most difficult part of a space mission, the launch. Beginning at the subsystem level up to the complete satellite, this environmental hazard must be considered in the design process.

Corrosion is an issue for LEO, where atomic oxygen can erode certain materials. Space debris is a concern for satellites at any altitude, but a collision is truly a rare event. In the context of this chapter, the main concern for missions where hundreds to thousands of satellites are deployed to perform a mission is the debris threat they pose to other systems. The only realistic way to solve this problem is to confine these missions to LEO, where the orbital lifetime is very short, essentially making these missions disposable. Currently, no de-orbit capability is planned for such small systems, due to the disproportionate size and mass requirements for such a system. The vacuum of space introduces several issues, such as cold welding and outgassing, but for very small systems, the main concern is limited heat transfer, i.e. keeping the satellite warm.

Thermal extremes and cycling are exacerbated on orbit in a vacuum, as thermal radiation is the only method available for heat transfer between the satellite and space. For some systems discussed in this research, bare silicon is proposed. For others, more traditional spacecraft structures are explored. In both cases, the key challenge is not overheating, but rather capturing and maintaining enough heat to operate correctly during the eclipse portion of the orbit.

Radiation and charged particles, whose fluence greatly varies with altitude, is one of the main problems addressed when flying COTS components in space [143]. Long-term exposure to radiation causes a degradation of performance and increased power draw due to the total ionizing

dose (TID) effect. This is not a great concern for short-lived missions in LEO, where the internal TID environment is only 1–1.5 rad (SiO_2) per day, which equates to an expected lifetime of at least 10 years. Coverglass is used to protect the solar cells. However, single event effects (SEE) must be tolerated and handled using various strategies. Single event upsets (SEUs) are the most common, where a logic bit is toggled. SEU rates of the order of 10^{-6} SEU bit^{-1} day^{-1} can be expected in LEO. Single event latchup (SEL) is more serious, as parasitic transistors in the circuit which are normally dormant can be activated pulling damaging levels of current, potentially causing burnouts [144]. The radiation environment is more fully explained in Section 5.3.1 with mitigation strategies discussed as needed in Sections 5.3.2 and 6.5.

Terrestrial sensor networks are composed of relatively fixed nodes. In contrast, orbital velocity in LEO is approximately 7.5 km/s. Natural, but undesirable perturbations change the orbit over time, altering the arrangement of nodes, or constellation in this case, as discussed in Section 3.3.4.3. This factor must be fully understood, so that key parameters like communication range can be selected properly. The freefall environment also presents unique challenges. The dominant effect is that objects in orbit "float" and change their orientation or "attitude" based on perturbations from solar pressure, gravity gradients, magnetic fields, and aerodynamic drag. This may not be an issue if the sensor technology does not have pointing requirements.

3.3.4.7 Launch and Deployment

Utilizing commercial launchers and existing deployment systems is essential to minimizing cost. Very small satellite deployment systems are increasingly used as discussed in Section 2.3.1.2, such as P-POD, T-POD, X-POD, SPL, and custom systems such as OPAL. The P-POD deployment system is shown in Figure 3-12. A model is shown on the left, with the containment door shut. The right side of the figure shows the post-deployment configuration, with the door open and ejection spring fully extended. P-POD is the selected deployer for this mission [71].

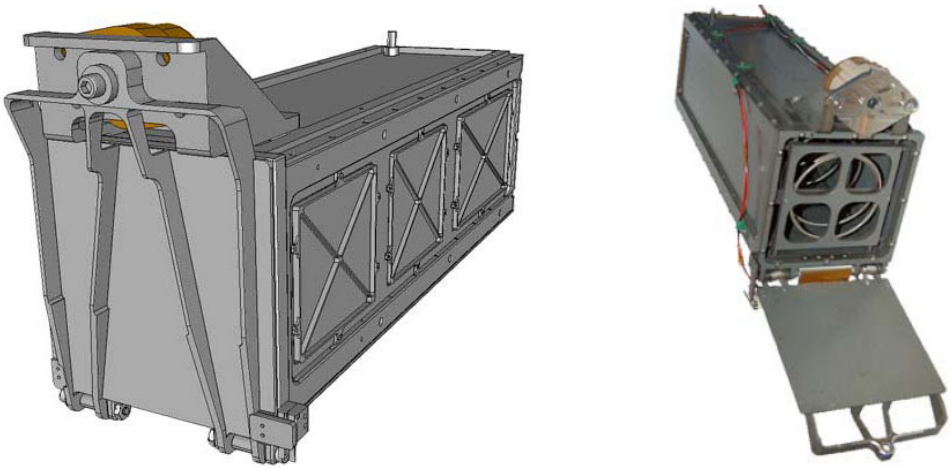

Figure 3-12. P-POD in Launch (left) and Deployed (right) Configurations [71]

NASA manages the Space Shuttle Picosat Launcher 5510 (SSPL) as shown in Figure 3-13. It can deploy a satellite or satellites with maximum total dimensions of 5×5×10 inches and 7 kg from the bay of the Shuttle [145]. This compares to the 3.94×3.94×11.8 inches, 3 kg capacity of P-POD.

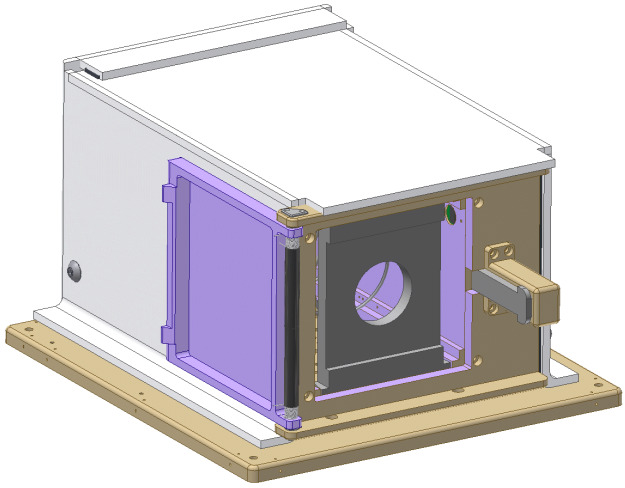

Figure 3-13. Space Shuttle Picosat Launcher 5510 (SSPL) [145]

Typically, only one or two P-PODs are mounted on a launch vehicle. SpaceAccess has developed the Secondary Payload Adapter and Separation System (SPASS), which can accommodate up to six P-POD compatible deployment systems as shown in Figure 3-14 [146].

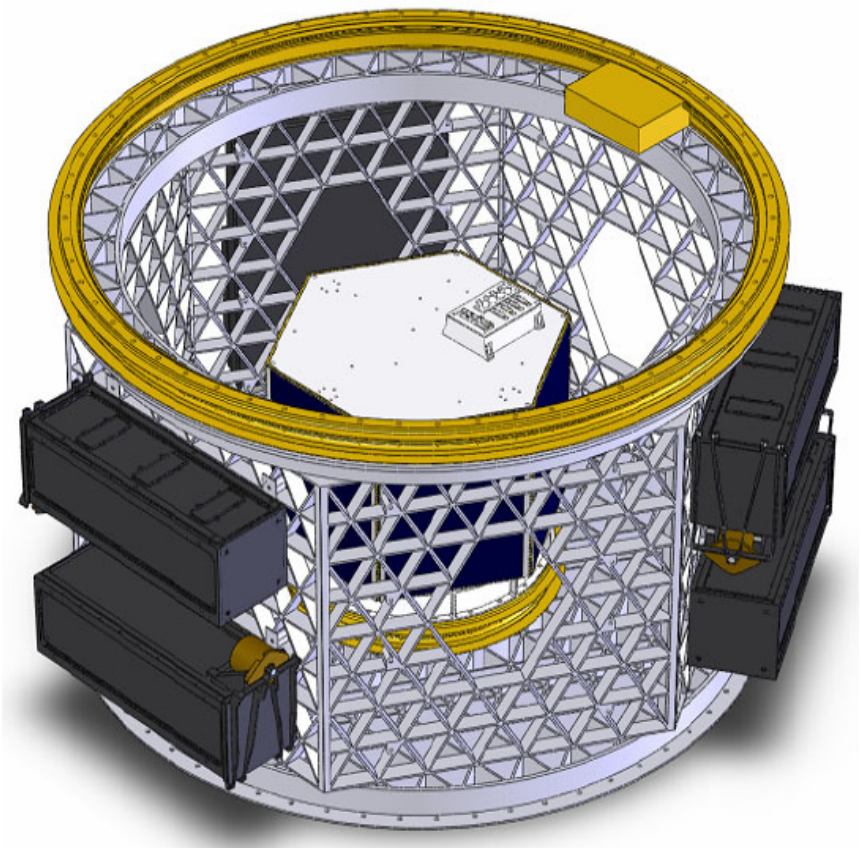

Figure 3-14. Secondary Payload Adapter and Separation System (SPASS) [146]

3.3.4.8 Mission Logistics

This mission is proposed from the onset as a short duration mission with as minimal financial and resources impact as possible. One primary concern when proposing the deployment of large numbers of satellites is the mitigation of orbital debris. Considering a maximum altitude of 500 km, the projected orbital lifetime is two and a half years as shown in Figure 3-15. The orbit apogee, perigee, and eccentricity are also shown in the figure.

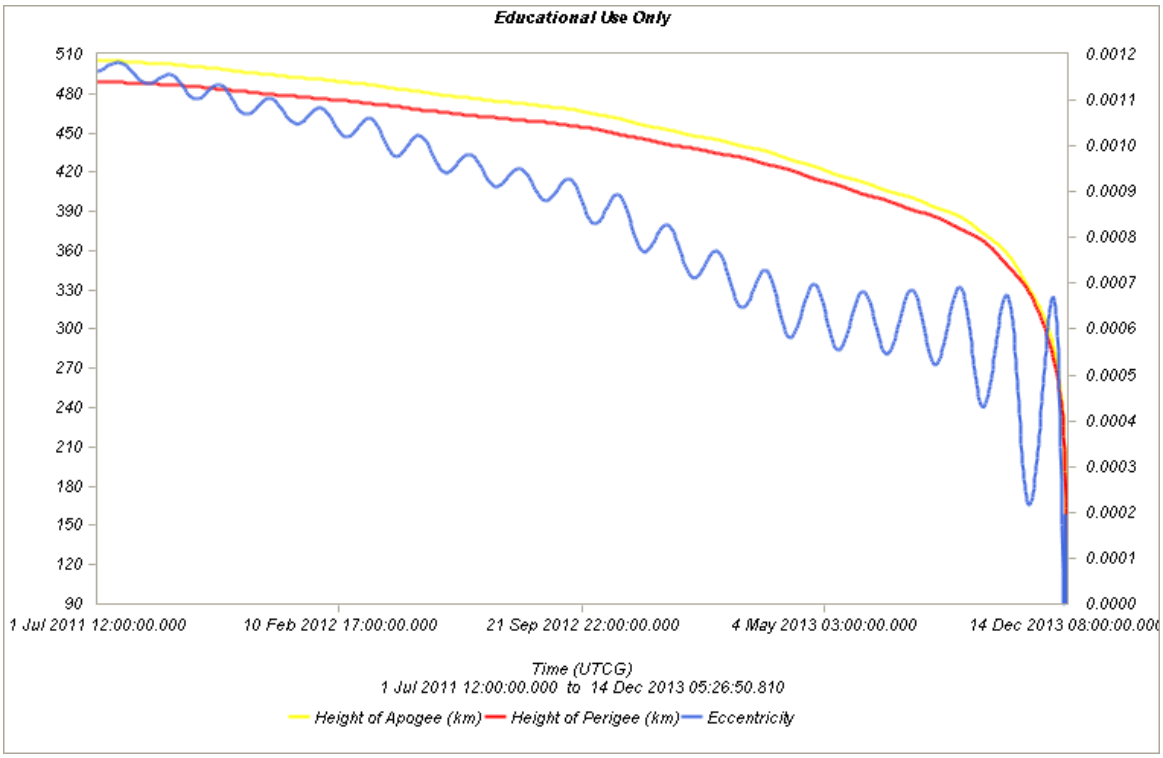

Figure 3-15. Mission Lifetime

3.3.5 Mission Evaluation and Requirements Definition

The final step in mission design is to translate the broad objectives and constraints presented in Table 3-3 into a detailed list of system requirements derived by the process outlined in Table 3-1. In this research, the focus is not on developing a specific implementation with a design project approach to meet the requirements of this particular case study mission. However, all technologies considered in Section 2.3 and presented in the remainder of this thesis are assessed for suitability to this case study mission. Specifically, the SpaceChip design methodology is assessed in Table 4-7, Chapter 4 and the PCBSat miniaturisation approach is assessed in Table 7-6, Chapter 7.

3.4 Summary

This chapter validates the claim that a basic space sensor network architecture can enable a meaningful user-driven scientific mission. An introduction is given to ionospheric plasma depletions, commonly known as plasma bubbles, which continue to plague satellite communication and navigation services with expected but inconvenient outages. A scarce few multi-million dollar satellites examine this atmospheric feature as a secondary mission at best, with the exception of the recently launched C/NOFS mission. A massively distributed mission conducting three-dimensional in-situ measurements can demystify this phenomenon.

Basic requirements are developed for a demonstration mission. An initial constellation of ten satellites is proposed, deploying from a COTS launch vehicle and deployer, and relying on atmospheric drag and solar radiation pressure to naturally distribute the constellation. Small variances in the satellite projected area and sunlit angle are suggested as low-effort physical solutions. Measurement campaigns will occur during the eclipse, where miniature plasma sensor data is recorded onboard once per second and time and position stamped by GPS. During the sunlit portion of the orbit, a co-orbiting, ballistic coefficient matched, master relay satellite will poll each satellite in the constellation using an ad-hoc, multi-hop mesh network. The master satellite can store numerous measurement campaigns, as the sensor data requirements are low. Using an amateur-class ground station, a single-eclipse data set can be downloaded in two passes. The lifetime of the mission will end at approximately four months, due to the communication range being exceeded between satellites. All satellites will re-enter within three years.

A challenging maximum budget goal for this demonstration mission is set at $500,000, which according to the numerous mission accounts in Section 2.2, is merely a fraction of any existing distributed satellite system. This sets the stage for an examination of very small satellite technologies, with the current state-of-the-art reviewed in Section 2.3. Two new very small satellite design approaches are now presented generically over the next four chapters, and then evaluated for cost-effectiveness and suitability to this specific case study mission.

Chapter 4

4 SpaceChip Feasibility Study

SpaceChip is a generic term coined in this research that describes the effort to define, assess, and develop the elusive design methodology of satellite-on-a-chip. A new dimension of system architecture design is emerging where hundreds to thousands of ultra-light (<10g) sensor nodes will collectively perform a spectrum of wireless sensor network missions in a distributed fashion. This scenario is analogous to a "smart" version of Project West Ford as discussed in Section 2.3.1.3. High volume production of sensor nodes at low cost is required to support this architecture. This chapter aims to assess a technique applicable beyond the space domain for designing and fabricating heterogeneous self-powered monolithic SoC wireless sensor nodes on commercially available CMOS processes. A brief introduction to the concept is given in Section 4.1. Sections 4.2 through 4.9 discuss state-of-the-art implementation possibilities for each required subsystem. Section 4.10 concludes with a feasibility assessment of satellite-on-a-chip.

4.1 Introduction

Since 1993, many have pointed to satellite-on-a-chip as the ultimate in spacecraft miniaturisation, proposing various hardware architectures and implementations [79]-[89]. In parallel, research and commercialisation of wireless sensor networks [3] and RFID [123] have developed many of the technologies that can now directly support SpaceChip. Therefore, in the context of this research, SpaceChip is literally defined as a monolithic sensor node implemented as a SoC targeted for sensor network scenarios in hostile environments, where all components are built on a single chip, without any packaging or external parts. The feasibility of this concept is presented based on Wertz and Larson's [11] SMAD principles.

The ultimate SoC vision for any application is a stand-alone product that can be used directly off the CMOS process line without any additional components, packaging, or interfaces. Figure 4-1 illustrates a notional SpaceChip system configuration. Any sensor node is typically composed of a payload and a set of supporting subsystems, including structural, electrical power (EPS), data handling (DH), communications (Comm), attitude/orbit control (AOCS), and thermal control (TCS). Some of these subsystems are not required for non-space applications, however all are considered in this research in order to completely cover the spectrum of potential environments.

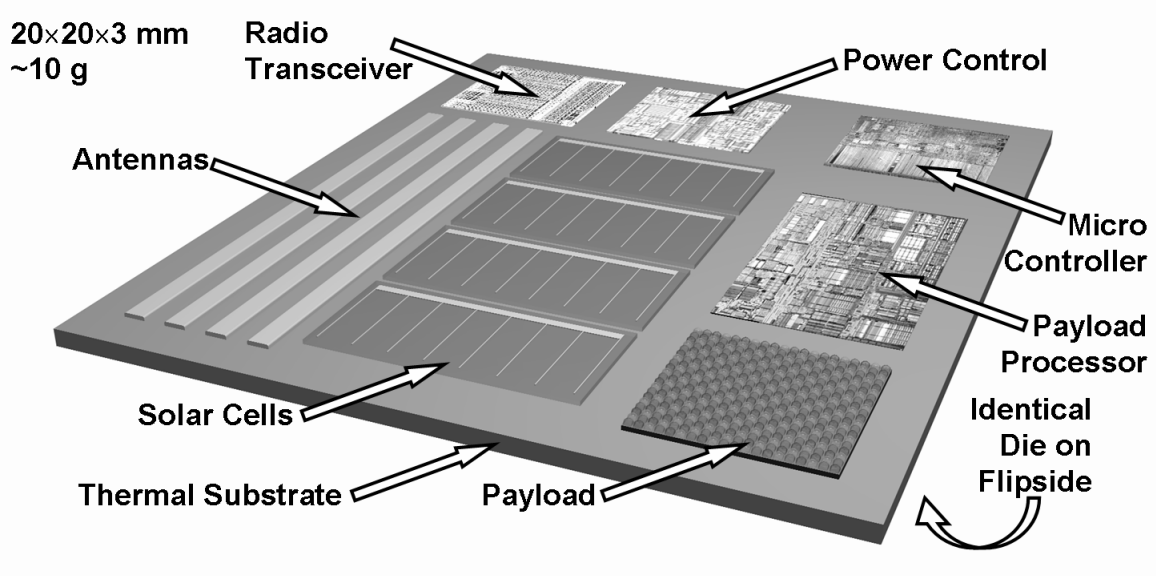

Figure 4-1. Notional SpaceChip System Configuration

4.2 System Configuration and Structure

Typical spacecraft design, detailed in Section 3.3, is driven by the required payload to meet mission requirements. With the payload defined, the configuration, which describes the physical relationship between the payload and subsystem components, can be developed. Subsystems are then integrated to support the payload's power, data handling, communications, attitude control, propulsion, and thermal control requirements. In the case of SpaceChip, the configuration is essentially fixed to the planar nature of a silicon chip.

CMOS technology is the most widely used microelectronics fabrication technology, due to its low cost at high volume. A maximum-sized prototype IC design, using a multi-project vendor such as MOSIS [147] or EUROPRACTICE [148], starts at $2,400 per die depending on the technology, whilst a production run would cost less than $300 each. Currently, feature sizes of 45 nm are possible, which will continue to shrink in time, but not without emerging challenges [149]. CMOS technology options have broadened over the past decade with the introduction of processes optimized for the integration of RF, optical, bipolar transistors (SiGe BiCMOS), and non-volatile flash memory components. SiGe BiCMOS offers demonstrated mixed-signal integration and is selected in this research as the technology platform [150].

The primary advantage of a monolithic approach is its manufacturing simplicity. However, it does not allow the attachment of discrete components or the merging of various elements into a hybrid assembly, which imposes considerable limitations. Most notably, the design cannot exceed the reticle size, which is a physical area limit imposed by the photolithography process used in the particular semiconductor process line. This caps the maximum circuit area to approximately 400

mm^2 (20×20 mm) for modern CMOS processes [149]. Assuming a silicon density of 2330 kg/m^3 and wafer thickness of 0.75 mm, the die mass is approximately one gram.

In 1967, wafer-scale integration (WSI) was proposed to overcome the reticle limit [151]. WSI enables multiple reticle-sized designs to be co-located on the same wafer, and then connected together using various interconnection techniques. The final product in theory could be as large as the entire wafer, which is currently 300 mm in diameter [149]. Unfortunately, inherent defects in the semiconductor manufacturing process have prevented WSI from becoming widely adopted [152], as a single wafer flaw would render an entire WSI system defective, greatly impacting yield. However, niche applications continue to emerge, including those for space [153].

MCM technology eventually replaced WSI for designs requiring more area [152]. MCMs integrate unpackaged "known-good-die" on a range of substrates, such as PCBs, thin films, and ceramics using fine line interconnects. MCM technology, including three-dimensional variants, has already been used in satellite applications [154]. MCMs or other system-in-package (SiP) techniques are typically used in applications where integrated density or performance is essential [155]. For less demanding applications, evolutionary advancements in IC packaging make traditional PCBs a cost-effective choice.

Despite the growing number of packaging alternatives, SoC technology is rapidly advancing. Popular MCM-based miniaturisation efforts, such as *Smart Dust*, are now looking to SoC for further miniaturisation of their terrestrial wireless sensors [121].

4.3 Payload

The chosen SoC approach greatly limits payload options. Considering the case study mission presented in Chapter 3, on-chip plasma sensors are not possible, due to the physical geometries required. However, sensors in Table 4-1 are routinely manufactured in CMOS [156].

Table 4-1. Typical CMOS Sensors [156]

▪ Visible	▪ Infrared	▪ Ultraviolet	▪ Electromagnetic
▪ Radiation	▪ Temperature	▪ Analogue input	

CMOS imagers are growing in popularity and may eventually replace charge-coupled devices (CCD) for most imaging applications [157]. Unlike CCDs, CMOS imagers use mainstream semiconductor fabrication techniques, require less power, and can be integrated monolithically with image co-processors. Complete camera-on-a-chip devices are now emerging [157]. Typically, a separate lens is required to focus the image on the sensor, but microlenses can now be integrated monolithically [158]. For the purpose of this feasibility study, a typical CMOS imager with a power requirement of 80 μW is used as a demonstration payload.

Recently, a wide range of sensors has emerged, based on *CMOS–MEMS* technology. CMOS–MEMS requires custom pre-, front-end, and/or back-end processing of the CMOS wafer. Of these three methods, back-end bulk micromachining of CMOS has been the most successful. Due to its growing popularity, a few commercial foundries now offer limited CMOS–MEMS processing, such as X-FAB [159]. Table 4-2 lists some sensors that have been demonstrated [160].

Table 4-2. Typical CMOS–MEMS Sensors [160]

▪ Pressure	▪ Chemical	▪ Thermal	▪ Tactile
▪ Proximity	▪ Flow	▪ Force	▪ Neural
▪ Vacuum	▪ Acceleration	▪ Gyroscopic	▪ Audio

4.4 Electrical Power Subsystem

Power distribution, regulation, and control aspects of an EPS can be met with basic wiring, switching, and regulation circuitry that are routinely implemented in CMOS [161]. Recent *micro power* research has presented several new integrated options for SoC applications, presented in Table 4-3 [162].

Table 4-3. Micro Power Sources [162]

▪ Solar cells	▪ Fuel cell	▪ Vibration	▪ Induction
▪ Chemical battery	▪ Nuclear battery	▪ Microturbine	

Power generation via integrated solar cells on CMOS is the most straightforward solution, but has not yet been demonstrated successfully. Typically, solar cells are fabricated with optimized silicon (Si) or gallium arsenide (GaAs) processes, optimized for efficiency and distinctly different from commercial CMOS. Integrating solar power with digital circuitry has not been of interest until recently. The first Smart Dust prototype was implemented as a MCM and attached to an external battery [116], then later used MCM integration to incorporate solar cells [117], and finally demonstrated a monolithic solution using a custom silicon-on-insulator (SOI) process [163]. Although SOI is growing in popularity, it is not yet commercially cost effective [164].

Truly monolithic self-powered devices in CMOS are rare. Four such examples are a sensor network processor [165], artificial retinal prostheses [166], and two generalized efforts [167]-[168]. These proposals rely on sub-threshold techniques, i.e. an operating voltage of less than 400 mV, as CMOS solar cells typically have an open voltage of 400-500 mV. Only [168] reports success in silicon, where a maximum of two cells in series, limited by inherent process limits, can provide up to 800 mV with an efficiency of 2.6%. Castañer discusses that most CMOS processes impose some restrictions that drastically reduce the efficiency of solar cells. His approach is similar to other efforts, using advanced packaging techniques to create self-powered SiP designs [169]-[170]. Obviously, with a maximum efficiency of 2.6%, integrated cells in commercial CMOS present a challenge. A novel solar cell design in SiGe BiCMOS is proposed in Chapter 5.

A monolithically integrated chemical fuel cell has been demonstrated with an operating time of 170 hours and mean open-circuit voltage of 0.533V [171]. Unfortunately, it relies on an oxygen-rich atmosphere, which is not suitable for space but will work terrestrially. In addition, no performance data under load is presented. Other micro chemical power supplies, such as thin-film batteries [172], nuclear batteries, and microturbines have been investigated, but none can be monolithically integrated.

Mechanical energy is typically converted by electromechanical generators, but piezoelectric power generation is also possible. Work is underway in piezoelectric micro power sources, but not yet for SoC [173]. Another promising source of integrated electrical power is through inductive energy transfer. This has been shown in a monolithic SoC for medical implants [174].

Using a baseline value of 80 μW for an example CMOS imager payload, Table 4-4 presents the notional SpaceChip power budget, which totals 1.14 mW, dominated by the communication subsystem, described later in Section 4.6. All other subsystem power requirements are based on the typical minimum values for small satellites [11].

Table 4-4. SpaceChip Power Budget

System	Typical [11]	Design	Units
Payload	40%	80	μW
EPS	20%	40	μW
DH	10%	20	μW
Comm	30%	1	mW
ADCS	0%	0	
Propulsion	0%	0	
Thermal	0%	0	
Structure	0%	0	
Total	**100%**	**1.14**	**mW**

With an initial power budget, the EPS sizing process is straightforward, using SMAD [11] equations. Equation (4.1) is first used to calculate an orbital period of 94.6 minutes. Assuming a circular orbit, the semi-major axis a is the sum of the 500 km altitude h and Earth radius $R_\oplus$ of 6378 km. The Earth's gravitational parameter $\mu_\oplus$ is a constant value of 3.986×10^5 $km^3 \cdot s^{-2}$. Equation (4.2) then gives an Earth angular radius ρ of 68 degrees.

$$P = 2\pi\sqrt{\frac{a^3}{\mu_\oplus}} \tag{4.1}$$

$$\rho = \sin^{-1}\left(\frac{R_\oplus}{R_\oplus + h}\right) \tag{4.2}$$

The results of Equations (4.1) and (4.2) give a time in eclipse T_e of 35.7 minutes as found with Equation 4.3. Subtracting this value from the period P results in a sunlit time T_s of 58.9 min.

$$T_e = \frac{2\rho}{360^\circ} P \tag{4.3}$$

A capacitor is assumed to be the only possible method of monolithic power storage. Using a 10% duty cycle of all systems during eclipse (~100 μW), a total power storage w requirement of 214 mJ is found from the product of the eclipse power requirement P_e and time in eclipse T_e. Equation (4.4) gives an integrated capacitance requirement of 68.5 mF for a 2.5 V process.

$$w = \frac{1}{2} C v^2 \tag{4.4}$$

Even using the high-capacitance option of 4.8 fF·μm^{-2} in SiGe BiCMOS, this would require an area of 40,000 times the maximum reticle area, conclusively ruling out integrated power storage. An external thin-film battery could be considered if required.

To determine the required solar array area, an average solar array output power requirement P_{sa} of 1.34 mW is found with Equation (4.5), assuming no eclipse operations (i.e. $P_e = 0$). The typical value of 0.85 is used for the sunlit power transmission efficiency X_s along with a sunlit power requirement P_s of 1.14 mW from Table 4-4.

$$P_{sa} = \left(\frac{P_s T_s}{X_s} + \frac{P_e T_e}{X_e} \right) / T_s \tag{4.5}$$

Finally, Equation (4.6) reveals a beginning-of-life areal power output of 24.4 W·m^{-2}. An average incidence angle θ of 45 degrees, solar flux G_s of 1326 W·m^{-2}, and no inherent degradation are assumed. A best reported efficiency η of 2.6% is used from [168]. The combined results of Eqs. (4.5) and (4.6) give an array size of 7.4×7.4 mm, which is only 14% of the maximum reticle area. This is a promising result, as much of the die area remains available for other subsystems.

$$P_{BOL} = G_s \eta I_d \cos\theta \tag{4.6}$$

One broad-scope issue that complicates the puritan satellite-on-a-chip idea is the resulting design is inherently two-dimensional, utilising only one side of the wafer. Such a configuration is problematic, as the system could go long periods without power if the inactive side faces the sun. Due to these physical constraints, a proposed deviation from the strict satellite-on-a-chip definition is considered. SpaceChip could be composed of two identical 20×20 mm die sandwiched together, with the active sides facing outward. No die interconnects would be required, as only one side at a time will be active due to solar illumination.

4.5 Data Handling Subsystem

The DH subsystem provides a range of on-board computing services. It receives, validates, decodes, and distributes commands from the ground, payload, or a subsystem to other spacecraft subsystems. It also gathers, processes, and formats spacecraft housekeeping and mission data for downlink or use on board. DH subsystems are usually the most difficult to define early in the design due to the initially vague requirements of the payload and subsystems.

At a minimum, the DH subsystem is composed of a central processing unit (CPU) and supporting memory elements. The difficult part of the design is the hardware interface to the other systems, typically using a digital data bus and analogue-to-digital converters (ADC). For SpaceChip, a minimal reduced instruction set (RISC) CPU design is all that can be supported by the available power. An on-chip ring oscillator with selectable frequency output and power up reset can be used to run the CPU. Some introductory thought has already been given to miniaturizing flight computer components to a single chip, reflecting a growing trend in SoC development [175].

One issue that plagues data handling systems operating in space is the extreme radiation and thermal environment, especially considering that the proposed system architecture is a bare die in space with no shielding. Additionally, low power operation is essential, considering the small surface area for integrated solar cells as discussed. A unique solution presented in Section 5.3 combines asynchronous logic and radiation hardening by design to enable low-power operation in most radiation environments.

4.6 Communications Subsystem

An obvious challenge for a satellite-on-a-chip is the communications link between the ground and the satellite. Due to its limited size, the onboard RF transmit power must be significant enough for an effective downlink. Initial calculations reveal that the corresponding electrical power to generate the minimum downlink RF power would require an integrated solar array area of at least 50 cm^2, which is much greater than the maximum reticle area. Tracking is another challenge, as the ground station must know the satellite's location exactly to avoid pointing losses with required high gain antennas. Due to the very small size of a satellite-on-a-chip, it is unlikely that space surveillance networks could detect it. The strategy to meeting these challenges is to avoid them altogether. A space sensor network architecture supported by a larger relay satellite is the suggested approach.

The original Smart Dust design presented in [116] uses optical communications to take advantage of its power efficiency. Optical links are also free of regulatory issues and can use simple on/off keying (OOK) modulation schemes. This approach is only effective in line-of-sight situations

where the alignment is controlled. For sensor networks within a larger spacecraft, line of sight would be difficult. For free-flying nodes, the alignment problem becomes the predominant issue.

Low-power on-chip transceivers have become the preferred choice for sensor nodes. SoC transceivers, which were a novelty only a few years ago are now commercially available, some even with an integrated microcontroller [176]. The commercial availability of RF CMOS and SiGe BiCMOS processes has offered increased capabilities, including a wider selection of operating frequencies. SoC transceivers still require external passive elements, crystal oscillators, and an antenna. In an effort to eliminate external antennas, on-chip antennas have been investigated. The maximum range achieved is approximately five metres, as demonstrated by Lin [177] and O [178]. Due to a 20×20 mm reticle size, most experiments use frequencies over 3.75 MHz, which gives a quarter-wavelength antenna size smaller than 20 mm. On-chip antennas for the 900 MHz and 2.4 GHz ISM bands are not feasible as they are 12.5 cm and 3.1 cm respectively. 5.8 GHz ISM fits well at 1.3 cm. Unfortunately, higher frequencies require more power given the same desired range than lower frequencies. RFID "tags" can be made monolithically, including an antenna, with a range of only a few metres [123].

The communication subsystem performance is determined as follows. Equation (4.7) gives a free space loss L_s of -100 dB for a range S of one kilometre. This assumes a 2.4 GHz ISM frequency, which has a wavelength λ of 12.5 cm.

$$L_s = \left(\frac{\lambda}{4\pi S} \right)^2 \tag{4.7}$$

Assuming no line, atmospheric, rain, or polarisation losses, the maximum bitrate R can be calculated using the simplified Equation (4.8) [179]. A solid state electrical to RF conversion efficiency of 1% gives a transmitter power P_t of 1 μW from an electrical power input of 1 mW as budgeted in Table 4-4. The transmitter G_t and receiver G_r gain are assumed to be unity, based on an off-chip antenna, as the on-chip results just discussed are prohibitive. A system noise T_{sys} of 21.3 dB·K [11] and Boltzmann's constant k with a value of 1.381×10^{-23} J·K^{-1} nearly complete the equation. Binary Phase Shift Keying (BPSK) modulation requires an energy per bit density E_b/N_o of 9.6 dB [11]. A bitrate R of 582 bps is found if assuming a +10 dB link margin. This limited range and bitrate ultimately emerges as the single most limiting performance parameter of SpaceChip concerning its applicability.

$$\frac{E_b}{N_0} = \frac{P_t G_t L_s G_r}{k T_{sys} R} \tag{4.8}$$

4.7 Attitude and Orbit Determination and Control Subsystem

The attitude and orbit control subsystem (AOCS) is composed of the attitude (ADCS) and orbit control segments. The ADCS keeps the payload, solar arrays, and/or high gain antennas oriented within a specified accuracy, whilst meeting range, jitter, drift, and settling time requirements. Small atmospheric, magnetic, gravitational, solar radiation pressure disturbance torques from the Earth and Sun complicate the problem. Various sensors and actuators are integrated into active or passive control systems. This becomes quite challenging on a chip scale.

Active ADCS, CMOS MEMS gyroscopes, magnetometers, and sun/horizon sensors are possible, but control options are limited to magnetorquers. A single chip magnetometer/magnetorquer ADCS has been demonstrated in [180]. Passive control is more realistic, where an aerodynamic *drag tail*, doubling as the external antenna, can be used in the drag environment of LEO. A magnetorquer could be used to further refine the control, as discussed in [181].

Orbit determination is very important to most missions. GPS has been acknowledged as an independent and reliable method for determining spacecraft position and velocity for small satellites. It is especially important to SpaceChip, as it may not be able to be tracked by conventional means and will need to report its position. Single-chip solutions are emerging, yet still require numerous large external passive components and up to 56 mW of power [182].

4.8 Propulsion Subsystem

Orbit control is nearly impossible without propulsion. Much work has been focused on propulsion for very small satellites. The most promising technology that may eventually be applicable is the digital micro-propulsion effort [183]. This technology requires a high activation voltage, has difficulty delivering symmetric thrust, and cannot be integrated monolithically with CMOS.

4.9 Thermal Subsystem

The temperature extremes a satellite-on-a-chip would experience are estimated with the following process. Using the previously calculated Earth angular radius ρ found in Equation (4.2), the flat plate over a spherical Earth configuration gives the corresponding view factors F_p = 0.86 and K_a = 0.99 using Equations (4.9) and (4.10).

$$F_P = \sin^2 \rho \tag{4.9}$$

$$K_a = 0.664 + 0.521\rho - 0.203\rho^2 \tag{4.10}$$

Assuming worst-case conditions, Equation (4.11) gives a maximum temperature of 96 °C. To calculate this result, a silicon absorptivity α_{Si} of 0.48, emissivity ε_{Si} of 0.46 [186], hot solar flux G_s of 1418 W·m^{-2}, albedo *alb* of 35%, and hot Earth infrared q_I of 258 W·m^{-2} [11] are assumed, along with the Stefan-Boltzmann constant σ of 5.67×10^{-8} W·m^{-2}·K^{-4}.

$$T_{\max(SA)} = \left[\frac{\alpha_t G_S + \varepsilon_b q_I F_P + \alpha_b a G_S K_a F_P - G_S \eta}{\sigma(\varepsilon_b + \varepsilon_t)} \right]^{1/4} \tag{4.11}$$

Similarly, Equation (4.12) gives a minimum temperature of -72 °C, using a cold Earth infrared q_I of 216 W·m^{-2} [11]. This temperature range is not unreasonable when compared to the operating range of industrial grade electronics (-40 to +85 °C). Further laboratory verification is needed and any problems most likely can be addressed with a simple phase-changing thermal management substrate, such as paraffin [184]. An investigation of the performance of the bipolar transistor feature of SiGe BiCMOS in extreme environments is reported in [185] with favourable results, however, the digital component is not discussed. Additionally, the asynchronous logic approach proposed in Section 5.3 is frequently used to enable digital devices to tolerate thermal extremes.

$$T_{\min(SA)} = \left[\frac{\varepsilon_b q_I F_P}{\sigma(\varepsilon_b + \varepsilon_t)} \right]^{1/4} \tag{4.12}$$

4.10 SpaceChip Technology Assessment

The concept of satellite-on-a-chip is assessed by the notional design approach of SpaceChip presented in this section. A summary of findings is given in Table 4-6, which highlights the area, power contributions, and requirements based on the best available reported results. Subsystem technology maturity is indicated by a technology readiness level (TRL) rating in Table 4-5 [187].

Table 4-5. Technology Readiness Level Definitions

1	Basic principles observed and reported
2	Technology concept and/or application formulated
3	Analytical and experimental critical function and/or characteristic proof of concept
4	Component and/or breadboard validation in laboratory environment
5	Component and/or breadboard validation in relevant environment
6	System/subsystem model or prototype demonstration in a relevant environment
7	System prototype demonstration in an operational environment
8	Actual system completed and qualified through test and demonstration
9	Actual system proven through successful mission operations

Table 4-6. SpaceChip Technology Assessment

Subsystem	Description	Area (mm^2)	Power (mW)	TRL	Reference
Structure	two die back to back	+ 400	-	2	this work
EPS	solar cells	- 55	+ 1.34	4	this work
Payload	CMOS visible imager	- 50	- 0.080	9	[157]
DH	MIPS microcontroller	- 0.5	- 0.05	4	this work
Comm	single-chip radio	- 36	- 1.0	9	[176]
ADCS	passive aerodynamic	-	-	9	[181]
OCS	single-chip GPS	- 23	- 56	4	[182]
Propulsion	digital micropropulsion	- 1 ea.	- 50,000	4	[183]
Thermal	paraffin or other	+ thickness	-	9	[184]

The fundamental purpose of this technology feasibility study is to determine if the elusive concept of satellite-on-a-chip can be made a reality. The key motivation of this approach is the potential very low cost of under $600 per satellite in massive quantities, recalling that two die are required in the space environment. The assessment reveals some encouraging complementary research in many areas, including micro power, sensors, wireless sensor networks, RFID, single-chip radio, on-chip antennas, single-chip GPS, and most surprisingly, chip-level propulsion systems. Although the concepts of satellite-on-a-chip and wireless sensor networks have existed since the early 1990's, only since 2005 have many of the enabling technologies come to fruition.

The key performance requirements and status are outlined in Table 4-7. The most limiting parameters lie within the power and communication subsystems.

Table 4-7. SpaceChip System Requirements and Status

System	Requirement	Outcomes
Top Level	▪Shall be implemented on a commercial CMOS process, suitable for integration of digital, analogue, and RF	▪AMS 0.35 μm SiGe-BiCMOS
Payload	▪The payload shall detect the phenomenon of interest ▪A simple demonstration payload shall be considered	▪Few options ▪CMOS Imager
Environment	▪SpaceChip shall operate in hostile environments	▪Tolerant to radiation and temperature
Configuration & Structure	▪Configuration shall be a monolithic "satellite-on-a-chip" ▪Size shall not exceed typical CMOS process reticle limit	▪20×20 mm ▪~10 g package
EPS	▪Power source shall be integrated solar cells ▪Secondary power storage shall be investigated	▪~1 mW budget
DH	▪Shall be based on a low-power simple microcontroller ▪Non-volatile memory technologies shall be investigated ▪Design shall withstand natural radiation environment	▪Hardened by design and asynchronous
Comm	▪2.4 GHz unlicensed ISM band shall be used ▪On-chip antennas too limiting, shall use external antenna	▪1 km range ▪582 bps
AOCS	▪Attitude determination shall not be required ▪Orbit determination options shall be investigated	▪Passive ADCS ▪GPS too much power
Propulsion	▪Propulsion shall not be required but shall be investigated	▪Not monolithic
Thermal	▪Passive control shall be used	▪Paraffin

A result of 2.6% efficiency of on-chip solar cells has been reported, but does not provide the required voltage level. More concerning is the potential communication range of one kilometre and half kilobit per second data rate. Additionally, no eclipse operations are possible as on-chip power storage is not feasible. Orbit determination is marginal as single chips are too small to track and single-chip GPS requires external components and too much power. Finally, chip-scale propulsion has been demonstrated, but the activation power requirements are too high and it cannot deliver symmetrical or reliable thrust. These limitations strongly suggest that the concept of SpaceChip is more suited to wireless sensor network applications in hostile environments where the communication range is sufficiently short. Numerous missions are possible in terrestrial, space, or interplanetary environments, however, the case study mission presented in Chapter 3 cannot be supported due to payload and communication requirements.

4.11 Summary

SpaceChip is a monolithic SoC approach under investigation to fabricate large numbers of wireless sensor nodes for hostile environments including space. A feasibility study is presented, featuring a generalized system architecture composed of a payload sensor and supporting subsystems implemented in SiGe BiCMOS. Conveniently, many of the supporting elements are currently being studied widely in the pursuit of ultra-miniature sensor nodes.

Chip-scale sensors are proliferating based on CMOS technologies, such as visible, IR, UV, electromagnetic, radiation, temperature, and analogue. Emerging CMOS–MEMS technology allows the monolithic integration of pressure, chemical, thermal, tactile, proximity, flow, force, neural, vacuum, acceleration, gyroscopic, and audio sensors. These sensors are frequently found with integrated data processing elements. More work is needed to integrate all required subsystems.

Micro-power generation and storage options, such as solar cells, fuel cells, vibration, induction, chemical batteries, nuclear batteries, and microturbines are the key enablers in energy harvesting applications, such as sensor networks. Unfortunately, induction is the only option that can be integrated monolithically. Integrated solar power has been attempted in CMOS, but has only been successful in SOI, which is not yet commercially cost effective.

Data handling is a straightforward application in CMOS, but environmental tolerance must be considered. Similarly, SoC radios with integrated data processing are now commonplace with a range up to one kilometre, but require external components and antennas. Integrated antennas have been demonstrated with a range of five metres. Position determination is now possible using SoC GPS solutions, but similar to SoC radios, they too require external components and consume too much power for any micro-power source. For applications in space, attitude and orbit control

may be required. Actuators have been demonstrated, but at the chip scale are very challenging and not yet practical. Finally, thermal control is relatively straightforward, with the application of passive thermal control substrates and asynchronous logic.

Until significant advances can be made, payload/sensor miniaturisation, power generation, and communication range will continue to be the most limiting aspects of the SpaceChip approach. These current limitations strongly suggest that the concept of SpaceChip is best suited for wireless sensor network applications in hostile environments where the communication range is sufficiently short. However, integrating as many spacecraft components as possible on one chip will always remain an elusive goal. Despite these limitations, two essential building blocks identified in this chapter are developed next in Chapter 5.

Chapter 5

5 Enabling Technologies for Heterogeneous SoC Design in Hostile Environments

Two essential building blocks are selected for further development and testing to support the vision of heterogeneous SoC sensor nodes for hostile environments. Section 5.1 links the research to the feasibility study discussed in Chapter 4. A new design for monolithically integrated solar cells in SiGe BiCMOS is presented in Section 5.2. Section 5.3 investigates a design approach that leverages radiation hardening by design and asynchronous logic to enable robust tolerance to radiation and thermal environments.

5.1 Introduction

Chapter 4 introduces and discusses the SpaceChip design approach, which is literally defined as a monolithic sensor node implemented as a SoC. Originally focused on satellite miniaturisation, SpaceChip encompasses any sensor network scenario in a hostile environment, where a low-cost mass-producible SoC solution is required. Enabling subsystems are further developed and tested in hardware as reported on in this chapter. Integrated solar cells and radiation hardening by design of asynchronous logic are two significant contributions to the SoC community.

5.2 Design of Monolithically Integrated Solar Cells in SiGe BiCMOS

As discussed in the SpaceChip feasibility study, solar cells are typically fabricated with dedicated silicon or gallium arsenide processes optimized for efficiency, then strung together externally with the appropriate series and parallel connections to achieve the desired voltage and current output. Regarding monolithically integrated cells, CMOS does not provide insulating features, as SOI, which facilitates series connections. Consequently, monolithic CMOS solar cell research is limited to a few attempts [165]-[167] with only one reporting partial success in silicon with an efficiency of 2.6% [168]. A novel approach to monolithic solar cell design in SiGe BiCMOS is presented here, which aims to overcome the limitations of these previous implementations. This technology development can be applied to a rapidly growing number of SoC applications.

5.2.1 Basic Solar Cell Theory of Operation

Solar or *photovoltaic* cells are devices that convert light energy or *photons* into electric current. Although modern day solar cells are derived from semiconductor technology made popular by the invention of the transistor in 1947, crude photovoltaic cells have been in use before 1900. The basis of a modern photovoltaic cell is the *p-n junction* of a crystalline semiconductor material, such as Germanium (Ge), Silicon (Si), Gallium Arsenide (GaAs), or numerous other compounds.

In silicon, for example, the p and n regions are created by introducing dopant materials, such as boron (B) or phosphorous (P), respectively. Boron has one less valence electron than silicon, so its introduction in the crystal lattice creates an absence of an electron, called a *hole* (+). Similarly, phosphorous has one more valence electron than silicon, creating an excess electron (-). The p-n junction is created from a single crystal. Under normal conditions, excess holes from the p-type material migrate to the n-type material whilst excess electrons in the n-type material migrate to the p-type material, where electron-hole recombination takes place until equilibrium is reached [188]. Under illumination, most of the photon energy is absorbed at the surface of the material, creating excess electron hole pairs reversing this migration process as illustrated in Figure 5-1.

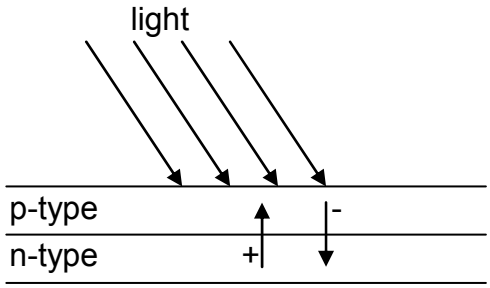

Figure 5-1. Illuminated p-n Junction Photovoltaic Effect

An ohmic contact is placed on each side of the p-n junction to harness the photovoltaic energy, as shown in Figure 5-2. The left side of the figure indicates the accepted voltage polarity convention, where the ground (gnd) probe of the voltmeter is placed on the n-type material and the positive (pos) probe is placed on the p-type material. Under illumination, the open circuit voltage is positive. On the right side of the figure, the short circuit current convention is illustrated, where the current flow is positive, indicating the flow of holes in the direction shown.

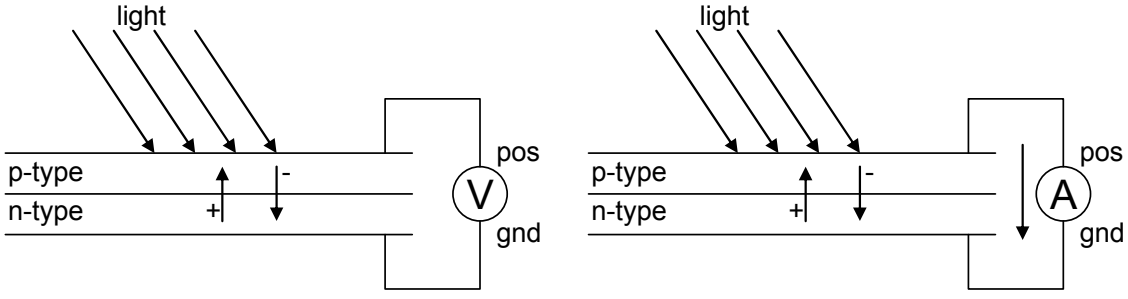

Figure 5-2. Photovoltaic Voltage and Current Direction Conventions

Due to the known limitations of integrated solar cells in CMOS, the literature is lacking in explaining why this direct approach does not work with useful experimental results. The first step in this research is the experimentation with CMOS solar cell designs. The 0.35 μm SiGe BiCMOS (S35) process from austriamicrosystems (AMS) is used throughout this work due to its common availability, cost effectiveness, lack of light-blocking layers, and support for integrated radio in future research. Nearly all CMOS-based processes use a p-type wafer, which is the substrate and typically used as system ground. Therefore, solar cells must be designed as shown in Figure 5-3, noting that the layer order is reversed from that presented in Figure 5-1 and Figure 5-2.

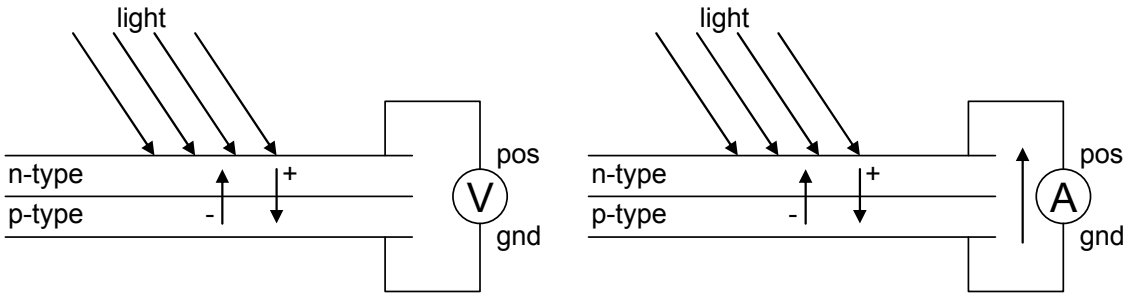

Figure 5-3. Standard Solar Cell Design in CMOS with p-type Substrate

Unfortunately, this approach has a few complications. Primarily, the bias with respect to ground is negative, which renders a self-powering approach impossible. Secondly, the solar cell voltage has a maximum of 500 mV open circuit, which is not very useful. Results reported in Section 5.3.4 show that designated 3.3V processes, such as AMS S35, have a minimum operating voltage of 900 mV. Integrated charge pumps [189] are an interesting consideration, as they can invert as well as raise voltage levels on chip. However, they too rely on a minimum start up voltage of 900 mV [190]. A recent SoC charge pump design for external solar cells is presented in [191].

5.2.2 Integrated SiGe BiCMOS Solar Cell Design

The n-p-n (NPN) SiGe bipolar junction transistor (BJT) structure is the primary reason for selecting the commonly available AMS S35 technology, as it provides a semi-isolated p-n junction at the surface. Not every detail of the AMS process is presented due to the academic non-disclosure agreement in force. Bulk CMOS only supports an n-well based n-p junction as discussed, which cannot provide series connections and produces a negative voltage with respect to ground, (the p-type substrate).

The novel photocell design utilizes NPN SiGe large area transistors, which are thin and close to the surface. The standard NPN SiGe BJT structure is modified to maximize the collector-base (C-B) interface and minimise the emitter (E) contact area which is left floating. A conceptual side view drawing (not to scale) is shown in Figure 5-4.

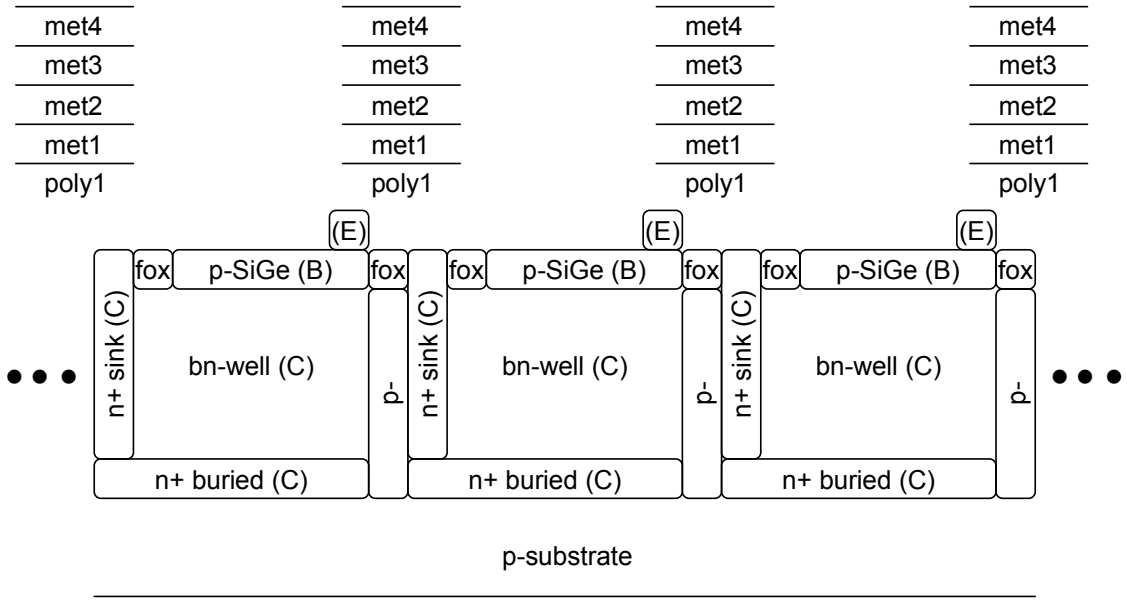

Figure 5-4. Photocell Design Concept (Side View)

A closer inspection of Figure 5-4 reveals the essential physical elements of the design. Starting from the bottom, the AMS S35 technology uses a typical p-type substrate. To create the collector (C), an n+ sinker and buried layer are required to contact the buried n-well. On top of the collector, the base (B) is formed of a thin p-type SiGe layer, where polysilicon (not shown) is used to make the base contact. Field oxide (fox) insulates the base from the surrounding elements. The emitter (E) is a small amount of n-type material connected by polysilicon (not shown) to create the complete NPN structure. The emitter is left floating and is kept as small as possible to maximize incident light whilst satisfying the process design rules. Finally, the polysilicon (poly1) through metal layer four (met4) are shown to illustrate that regular placement of these layers is required to satisfy the coverage and slotting rules of the process. Unfortunately, these layers reduce the overall efficiency dramatically.

The advantageous placement of field oxide in the NPN design is what makes series connections possible in SiGe BiCMOS and not bulk CMOS. Making the series and parallel cell connections is straightforward with this single-cell design. As shown in Figure 5-4, these cells are arranged for a series connection, raising the voltage at each increment. The base (B) of one cell is connected to the neighbouring collector (C) through vias to the metal layers above (not shown). Viewing the cell design from the top, Figure 5-5 illustrates how the field oxide completely isolates the p-type SiGe base (B) from the adjacent material. However, this design is not as efficient as a similar one in SOI, as there is no insulating layer available between the bottom n+ buried layer and the p-substrate as shown in Figure 5-4. Figure 5-6 illustrates the physical layout in the Cadence computer aided design (CAD) software tool, mirroring the view in Figure 5-5.

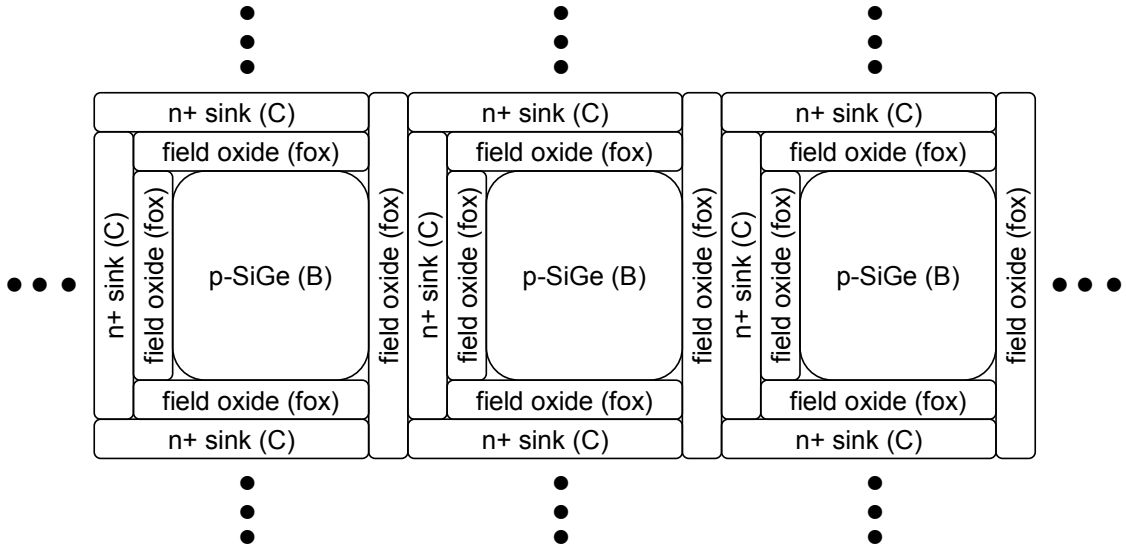

Figure 5-5. Photocell Design Concept (Top View)

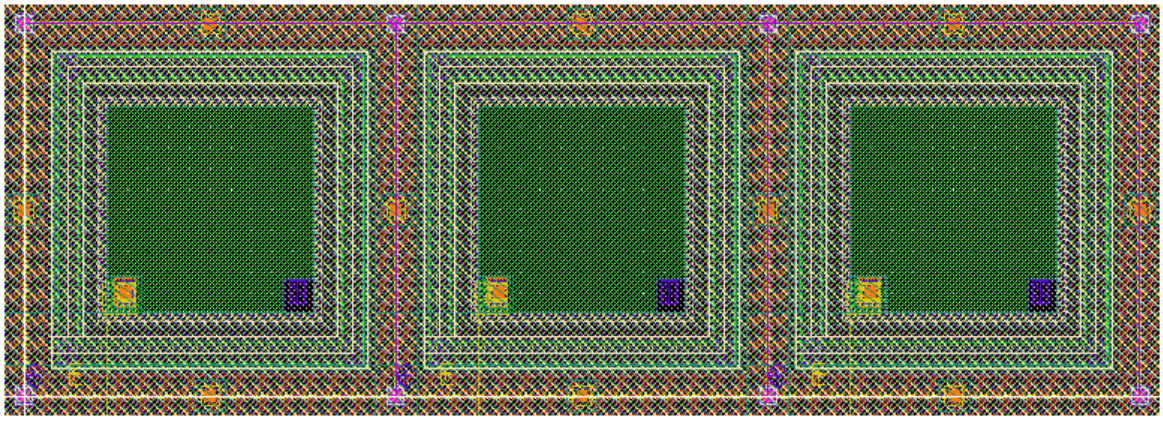

Figure 5-6. Photocell Design Concept (Cadence Layout View)

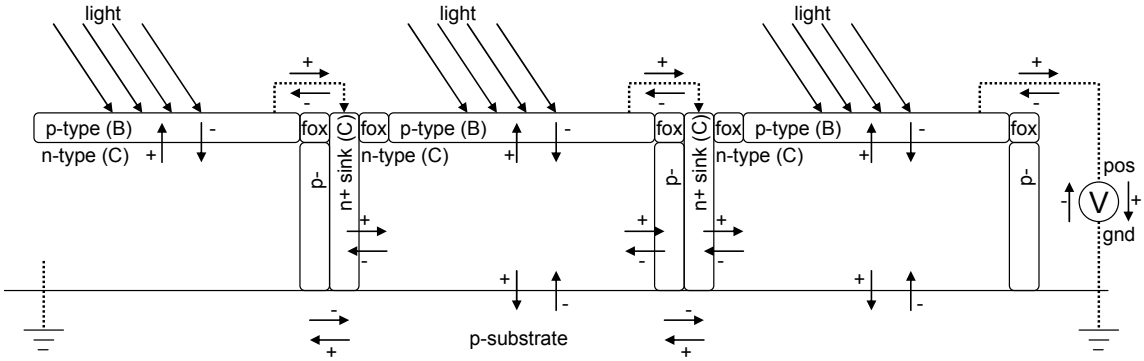

Figure 5-7. Photocell Design Concept (Schematic View)

Figure 5-7 is a hybrid view of the layout and schematic. It is essential to understand that whilst most light is absorbed at the top layer, some penetrates into the material and activates the lower n-p junction at the substrate as well as the n-p junction of the sidewalls. All electron hole migrations are illustrated, giving the desired elevated positive bias with respect to the substrate.

5.2.3 Integrated SiGe BiCMOS Solar Cell Test Results

Figure 5-8 illustrates the layout in Cadence of the first test chip from run 1550 on the left. The right of the figure shows the micrograph of an unpackaged die after fabrication (1420×1420 μm).

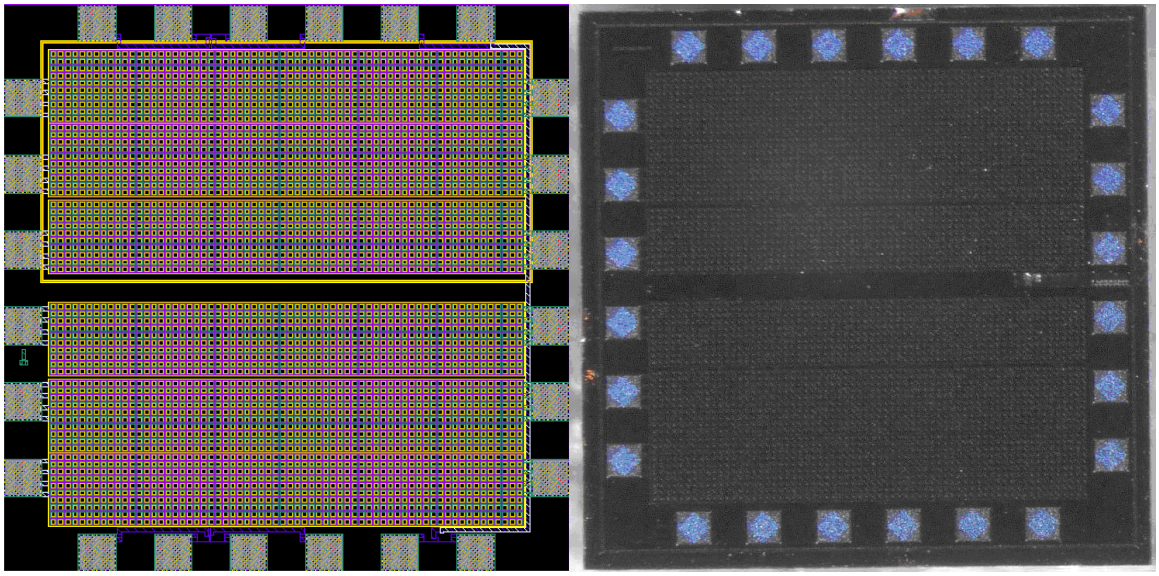

Figure 5-8. Test Chip #1 Layout (left) and Micrograph (right)

The schematic of the design is similar to that in Figure 5-7; however, the base (instead of the emitter) is erroneously floating on each cell, referencing a photocell design given in [157]. Secondly, there are six banks of photocells in parallel, three on the top and three on the bottom, with a large channel in between the sets and smaller channels within the sets of three. Additionally, the six banks of photocells have all collectors (left) and emitters (right) connected to the adjacent test pads. This allows for external series connections of the cells.

Test chip results reveal that the NPN CB junction is not activated as expected. Upon closer investigation, the reference photocell design [157] is not appropriate for this application as the B-E interface acts as a diode, preventing current from flowing through this interface. However, the test chip allows examination of the underlying n-well to p-substrate junction. The performance result has some value, as efficiency from this straightforward approach is not reported in the literature. As described and expected, this junction has a negative bias with respect to the substrate, which prevents direct application of the power from the cells to the IC.

Solar cells from AMS S35 run 1550 test chips are subjected to AM0 solar conditions per American Society for Testing and Materials (ASTM) International E-490 (1366.1 W/m^2) [192]. Summary current and power measurements are presented in Figure 5-9 for five devices. The average efficiency is 2.4%, closely matching the 2.6% from previous work [165]. The actual efficiency of the interface is 8.3%, without considering the metallisation overhead.

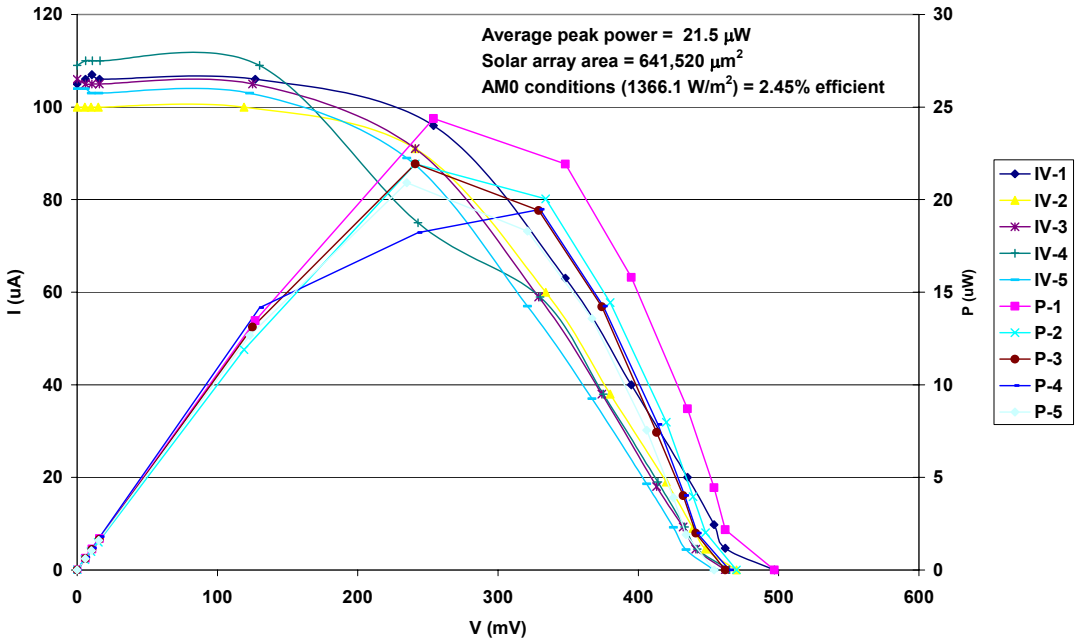

Figure 5-9. Solar Cell Current vs. Voltage, AM0, Test Chip #1

As the cause for the unexpected results was not immediately discovered, further examination of n-well based photocells took place. To potentially improve efficiency, the SiGe layer shown in Figure 5-4 are removed to allow more light to penetrate down to the lower n-well junction. The improved cells are included with other work on run 1791, Test Chip #2AR, discussed in Section 5.3 and can be clearly seen around the padframe in Figure 5-10. They demonstrate 3.44% efficiency as shown in Figure 5-11, which is a 40% improvement over the first attempt. The interface efficiency alone is 11.3% without considering the metallisation overhead.

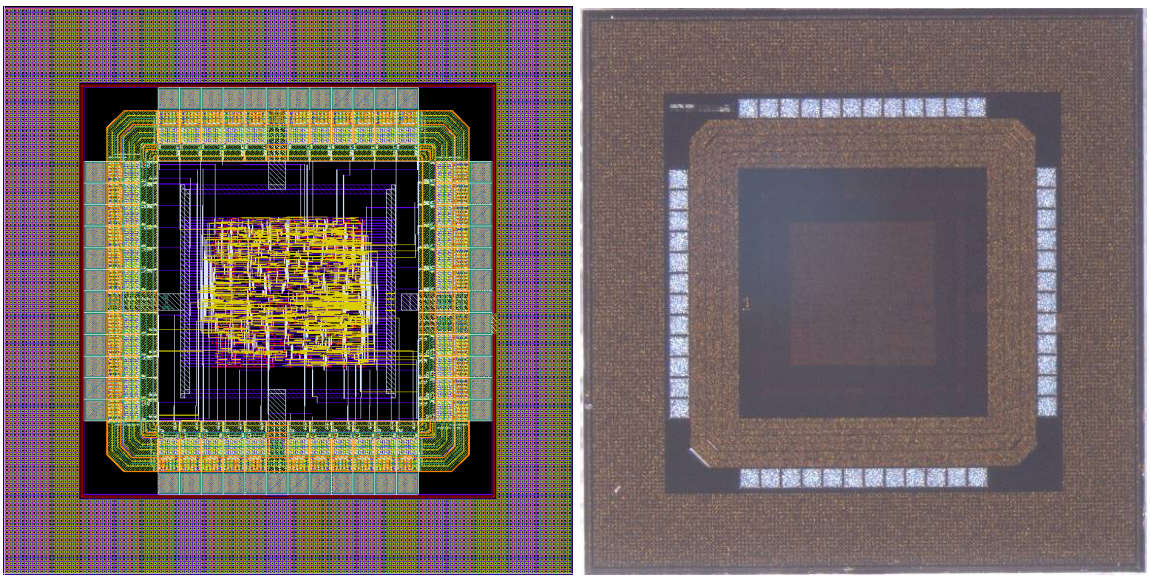

Figure 5-10. Test Chip #2AR Layout (left) and Micrograph (right) Shown with Solar Array

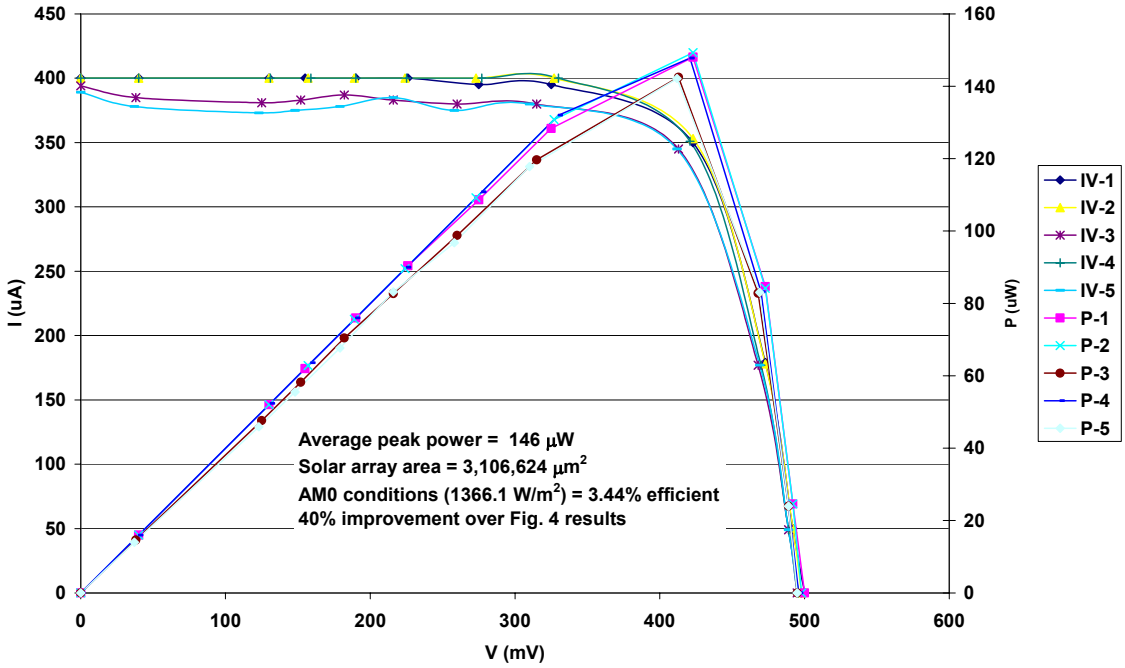

Figure 5-11. Solar Cell Current vs. Voltage, AM0, Test Chip #2AR

With the corrected SiGe BiCMOS design as shown in Figure 5-7, Test Chip #3 is fabricated on run 1875, with the layout and micrograph shown in Figure 5-12, which intended to provide a positive bias with respect to the substrate and selectable voltage. The lower right test point is ground (p-substrate) and the lower left point gives the bias across the first bank of cells in parallel. The remaining test points allow the measurement of successive banks in series. There are 18 banks in series, each with 264 cells in parallel.

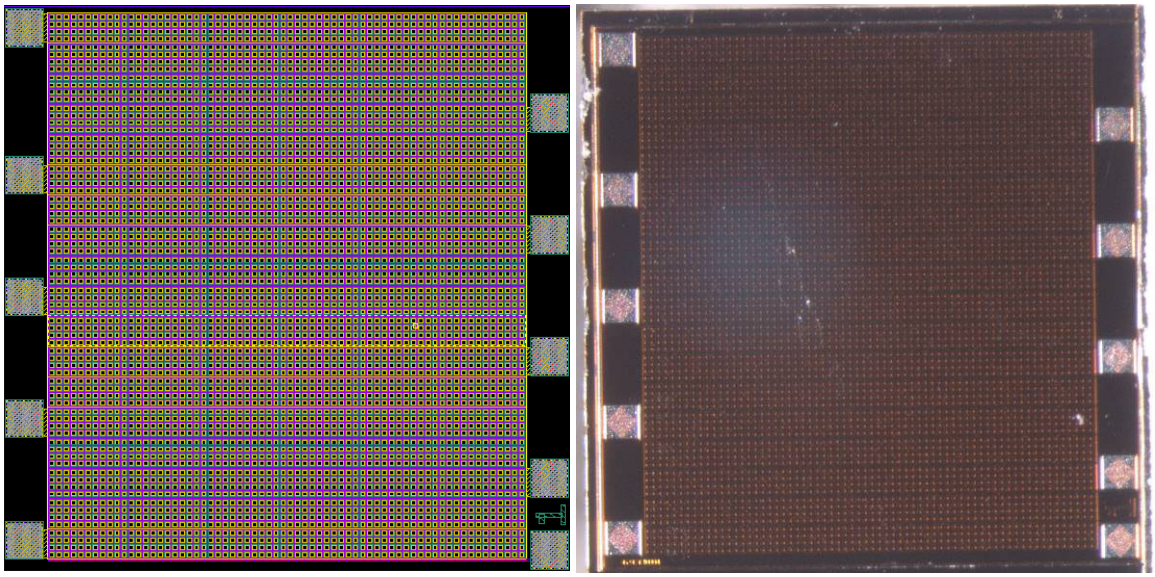

Figure 5-12. Test Chip #3 Layout (left) and Micrograph (right)

Test Chip #3 demonstrates an efficiency of 2.1% as shown in Figure 5-13. Although the efficiency is less than expected, this can be the result of fabrication process and test fixture variations. Unfortunately, the more important aspect of positive bias and on-chip series connections cannot yet be demonstrated. More investigation of this promising approach is required to determine why the hardware results do not match the expected theoretical results.

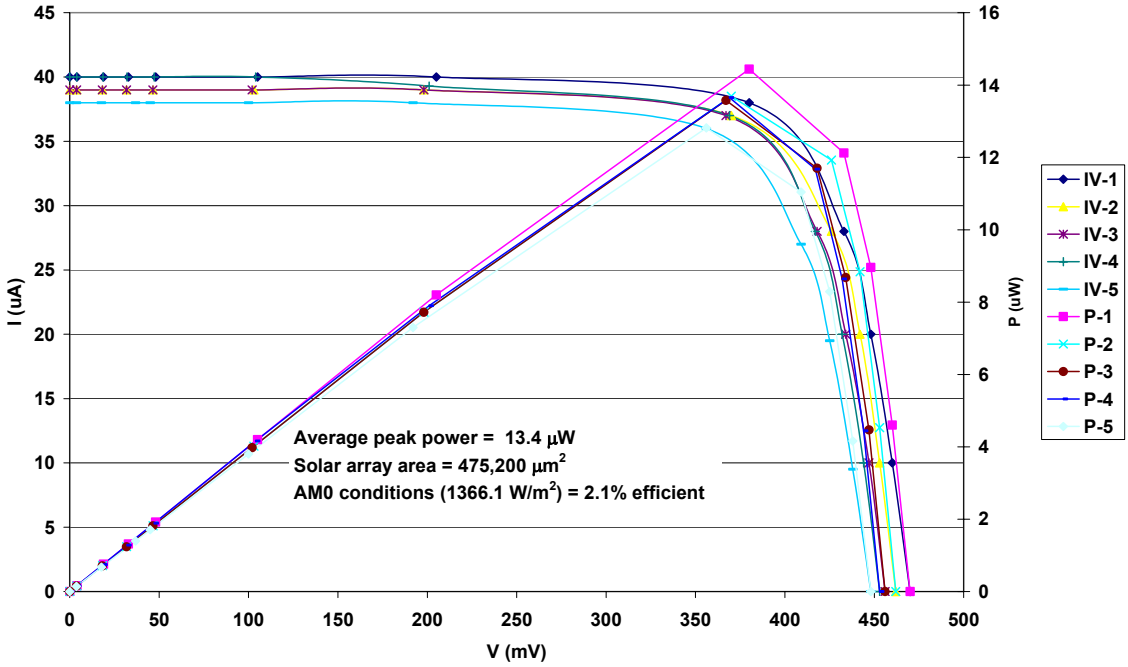

Figure 5-13. Solar Cell Current vs. Voltage, AM0, Test Chip #3

5.3 Radiation Hardening by Design of Asynchronous Logic

A novel case study supporting the development of a SpaceChip DH subsystem is presented. The synergy of radiation hardening by design (RHBD) of asynchronous logic improves the tolerance to radiation, semiconductor processing variations, voltage fluctuations, and temperature extremes. RHBD has been recognized for over a decade as an alternative open-source circuit design approach to mitigate a spectrum of high-energy radiation effects, but has significant power and area penalties. Similarly, asynchronous logic design offers potential power savings and performance improvements, with a tradeoff in design complexity and a lesser area penalty. These side effects have prevented wider acceptance of both design approaches.

5.3.1 Radiation Hardened by Design Background

Extreme radiation conditions are usually experienced in nuclear power plants, some industrial process plants, and in space. Surprisingly, in the early days of IC development, alpha particles

from impurities in plastic packaging caused mysterious anomalies in terrestrial systems. Neutrons occasionally cause errors in airplane avionics systems flying at normal cruising altitudes [144]. Space and various nuclear environments are more challenging, where the TID of radiation causes gradual system degradation, resulting in an increase in power consumption. In addition, high-energy particles, such as electrons, protons, and heavy ions/galactic cosmic rays (GCRs), can cause SEE, predominantly SEU, SEL, and recently, singled event transient (SET). Unnatural effects, such as enhanced dose rate, prompt neutron dose, and system electromagnetic pulse (EMP) are not discussed, as they are only concerns for hardened military systems.

Mitigating these effects has historically been accomplished with a system-level approach and can become quite expensive. Heavy shielding of various types can be used to reduce TID and system EMP, but is ineffective against SEE. SEE are tolerated and detected, typically through triple (or more) modular redundancy (TMR) or voting schemes. At the IC level, dedicated semiconductor foundries for military purposes only are used to produce hardened components. These hardened foundries are typically several generations behind their commercial counterparts. One accepted radiation-hardening solution at the IC level is the application of RHBD [193], which can be used on any generation process including the most recent. The guiding principle behind RHBD is to mitigate as many of the radiation effects as possible by using unconventional layout techniques at the transistor device and circuit level.

Beginning with TID, the degradation mechanisms must first be understood before they can be mitigated. CMOS circuits slowly degrade due to the total accumulated dose of ionizing radiation. This degradation is seen as a negative shift in the transistor threshold voltage and decrease in gain. With enough voltage threshold shift, leakage currents will greatly increase. The decrease in gain causes the transistors to become more difficult to switch. After extended exposure to radiation, the circuit will cease to function [194]. The main source of degradation comes from the interaction of ionizing radiation with the gate and field oxides (SiO_2) in the device structure. The gate oxide is a thin high-quality oxide used to insulate the gate contact from the transistor channel. The field oxide is a thick low-quality oxide used to isolate metal traces from one another [144].

Ionizing radiation causes the formation of electron-hole pairs in the gate oxide. Electrons have a much higher mobility than holes in SiO_2 and are attracted to and swept out of the gate in an n-type (nMOS) transistor. The holes become trapped and migrate toward the transistor channel. This results in the eventual build-up of positive charge above the transistor channel and resembles the charge that is present when voltage is applied at the gate. As more charge is trapped, the voltage threshold of the nMOS transistor becomes increasingly negative, which means it becomes easier to activate. With enough shift in threshold voltage, the transistor will be activated without gate bias applied. Conversely, a pMOS transistor becomes more difficult to activate, but is not as

sensitive to TID. Figure 5-14 shows how the gate voltage versus drain current curve changes resulting from exposure to radiation in an nMOS transistor [144].

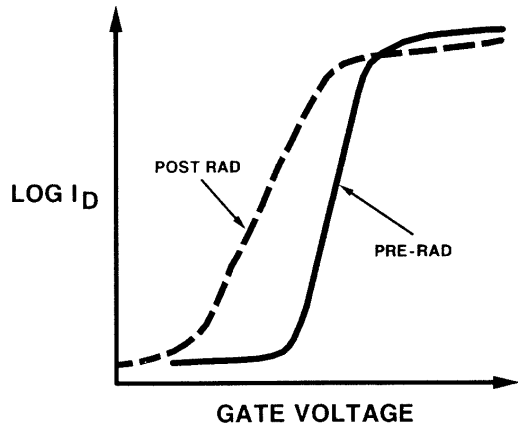

Figure 5-14. Total Ionizing Dose Effect on nMOS Threshold Shift [144]

The field oxide also traps charge due to ionizing radiation. The trapped positive charge along the edges of the nMOS transistor creates a leakage channel. Leakage paths can also form between transistors through the field oxide. This constant leakage contributes to increased power consumption [144]. Figure 5-15 illustrates how a circuit exposed to a radiation environment slowly increases power consumption and reduces the operating frequency. Eventually, the circuit will cease functioning when the power required by the degraded electronics exceeds the output capability of the power supply. Premature failure can also occur when the output voltage swing of the transistors becomes insufficient to drive successive stages or when the timing is degraded to the point where the circuit does not operate properly.

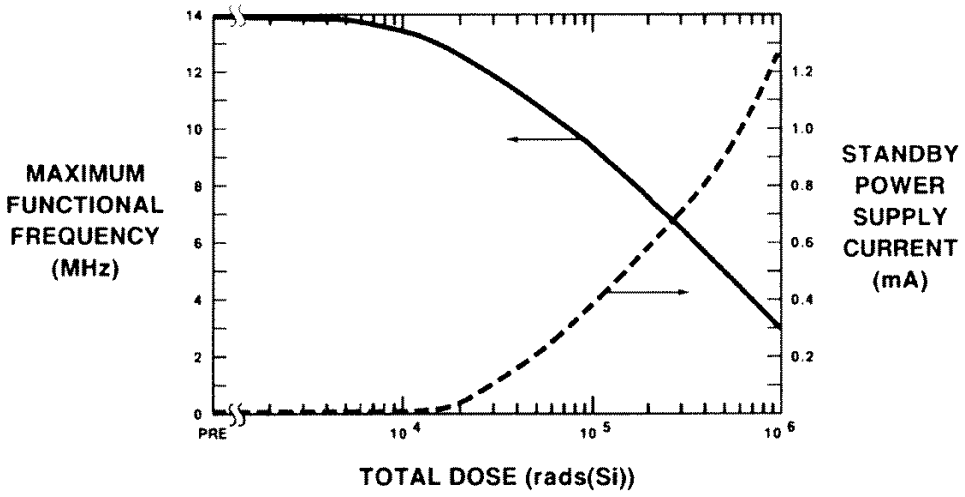

Figure 5-15. Total Ionizing Dose Response of Maximum Frequency and Supply Current [144]

When a high-energy particle passes through a circuit and causes a disruption in circuit operation, it is classified as an SEE. For example, a proton or heavy ion passing through a latch could change the value of a stored bit, which is called an SEU. Space vehicles passing through the South

Atlantic anomaly, where there is a high concentration of protons, typically experience high SEU activity in that region. These particles create a temporary presence of an abundance of free carriers in the transistor channel region. The free carriers in effect turn the channel on.

If a channel is activated in a combinational logic circuit, the effect is seen as a glitch in a data or control line, which normally does not affect system operation unless the glitch occurs during a clock transition. However, if a channel is activated that is part of a memory structure, such as a latch, it can change the state of the latch. Upset can only occur if enough carriers are present in the transistor channel to turn it on strongly enough to change the state of the latch. SEU can be corrected by refreshing memory locations on a periodic basis.

Another effect seen in CMOS is SEL. SEL describes the phenomenon that occurs when inactive parasitic transistor regions (p-n-p-n structure) are turned on by a high-energy particle. These p-n-p-n regions are formed in CMOS layouts due to the close placement of nMOS and pMOS transistors and have the characteristics of a silicon controlled rectifier (SCR). If a particle with enough energy passes through the controlling p-n junction of the SCR, it can switch the SCR on. The only way to turn the SCR off is by cycling the power.

5.3.2 Radiation Hardened Library Design

An RHBD digital cell library is designed for the AMS S35 process (HITKIT 3.70) in the Cadence DFII framework (2006-2007 5.1.41). The creation of this library is essential to this work, because RHBD libraries are not freely available, as they are regarded as intellectual property and are usually foundry process dependent. Radiation tolerance to TID and SEE is achieved through layout [193]. RHBD libraries generally use a sea of gates or gate array approach with a base transistor pair. The base transistor pair developed in this work is shown in Figure 5-16. Total ionizing dose effects are minimised by the use of annular geometry nMOS transistors. This geometry minimises the threshold voltage shift preventing the build-up of trapped charge near the active region and eliminates edge leakage. The transistors are surrounded with highly doped guard rings, which prevent leakage through the field oxide separating the transistors and nearly eliminate SEL. The inherent increased drive strength (width) of the transistors, due to meeting minimum design rules for the annular nMOS then balancing with pMOS, increases the SEU threshold and reduces SET. The drawback of the gate array approach is the increased area whilst the annular nMOS and matched pMOS directly contribute to the increased power requirements.

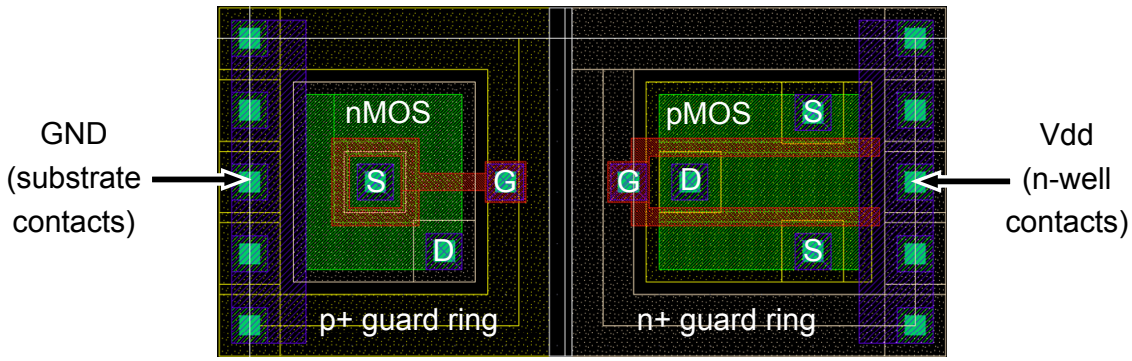

Figure 5-16. RHBD Layout of Core Transistor Pair

The actual layout and geometry of the transistor pair is driven by minimum process design rules. The height and width of the base pair is governed by compatibility with the place and route tool. Some designs use two pairs of transistors within guard rings, but for this investigation, only one set is used [195]. One typical complication of RHBD libraries is that the transistor parameter extraction tools, including Cadence Assura, do not properly determine the annular transistor parameters [196]. Specifically, they cannot accurately calculate the transistor length, width, source area, source perimeter, drain area, and drain perimeter. These must be calculated by manually measuring the design. The initial approach taken in this work is to edit the extraction rules file and modify the equations. However, this only covers the length and width, as the area and perimeters are determined by another process not modifiable by the user. Ultimately, the extracted netlist is modified by a simple search and replace script based on expected erroneous values and correct values.

As CMOS technologies mature, the minimum feature size continues to shrink, which is currently at 45 nm [149]. Recently, annular transistors have received new attention as a technique to improve circuit reliability for mission-critical systems using the newest CMOS technologies. Furthermore, the work in [197] demonstrates through experimentation and test that by choosing the interior contact of the nMOS as the source (S), the reliability is further enhanced. This approach is used in the library developed in this research. Reliability is degraded when the interior contact is chosen as the drain. This is an interesting result, as most existing designs use this configuration.

Numerous RHBD efforts have demonstrated considerable radiation hardness. As long as the basic approach is followed, the hardness of the library developed in this work should be comparable to similar libraries. For example, a recent design and test campaign in 0.25 μm CMOS achieved these results, which far exceed envisaged SpaceChip mission requirements [198]:

- TID > 1 MRad (Si)
- SEL > 110 MeV-cm²/mg @ 125 °C (latch-up immune)
- SEU < 1x10-12 errors/bit-day @ 2.25V

A simplified overview of the library development process is presented in Table 5-1. Each step involves a significant time investment due to the required learning curve of the complex, yet powerful, commercial tools involved. The simplest cell in the library is the INV0 with the most complex being the DFP1 as compared in Figure 5-17. Step 6 of Table 5-1 requires the most effort, as each cell must be routed manually whilst conforming to the design rules. Metal 2 is the highest metal layer used in any cell, with most cells being routed primarily with only Metal 1. Library characterisation, through tools such as Signal Storm is intentionally not accomplished, as RHBD libraries are ideally suited as a one-to-one replacement of standard commercial cells. The justification is that RHBD cells have a much higher drive strength, which contributes to SEU and SET hardness. The various optimisation stages would incorrectly increase fanout with a matching timing library, thereby lowering the SEU hardness. Using the commercial timing library with RHBD layouts prevents this problem. Whilst hardware description language (HDL) simulations are not ideal in this situation, extracted layout simulations confirm proper timing and performance before fabrication. A complete list of cells required to complete all designs are listed in Table 5-2 and Table 5-3.

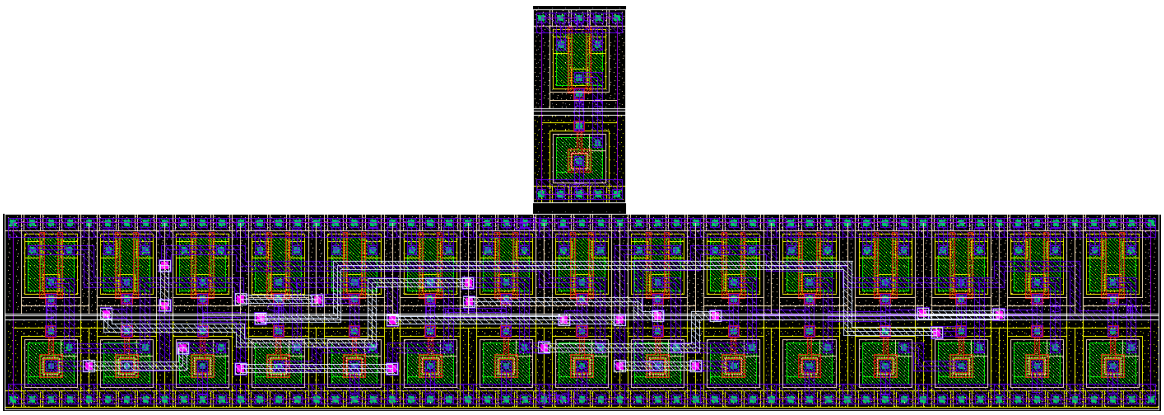

Figure 5-17. Comparison of Smallest Cell (INV0, top) with Largest (DFP1, bottom)

Table 5-1. Radiation Hardened Library Design Development Process

Step	Tool	Action
1	Library Manager	Copy CORELIB, GATES, IOLIB, and PRIMLIB to *_RHBD
2	Virtuoso (Pcell)	Create/compile nmos4 and pmos4 pcells in PRIMLIB_RHBD
3	CDF	Edit descriptions of nmos4 and pmos4 in PRIMLIB_RHBD to match
4	Virtuoso (Schematic)	Verify/update width and length parameters in GATES_RHBD
5	Virtuoso (Schematic)	Design synthesis to Layout XL
6	Virtuoso (XL)	Manually place and route pcells, label terminals
7	Assura	Copy/edit extract.rul file to extract annular nMOS properly
8	Assura (DRC)	Run design rule check, correct errors as needed
9	Assura (LVS)	Run layout versus schematic, ensure designs match
10	Assura (RCX)	Run parasitic extraction and verify av_extracted view
11	DFII (Export Stream)	Create gdsII files from layout view
12	Library Manager	Create functional (Verilog)
13	Abstract Generator	Complete abstract generation process for each cell
14	Virtuoso (Layout)	Manually convert nMOS devices in IOLIB to equivalent annular
15	Voltage Storm	Characterize and create timing libraries for Verilog and Encounter

Table 5-2. Radiation Hardened Library Core Cells

Cell	Description	Standard Size (μm)	RHBD Size (μm)
AOI210	2-Input AND into 2-Input NOR	5.6×13	16.8×13
AOI220	2x2-Input AND into 2-Input NOR	7×13	22.4×13
AOI310	3-Input AND into 2-Input NOR	7×13	22.4×13
BUF2	Buffer	4.2×13	11.2×13
DF1	D Flip Flop	21×13	67.2×13
DFC1	D Flip Flop w/active low clear	23.8×13	78.4×13
DFP1	D Flip Flop w/active low preset	23.8×13	78.4×13
INV0	Inverter	2.8×13	5.6×13
MUX21	2:1 Multiplexor	8.4×13	33.6×13
NAND20	2-Input NAND	4.2×13	11.2×13
NAND30	3-Input NAND	5.6×13	16.8×13
NAND40	4-Input NAND	7×13	22.4×13
NOR20	2-Input NOR	4.2×13	11.2×13
NOR30	3-Input NOR	5.6×13	16.8×13
NOR40	4-Input NOR	7×13	22.4×13
OAI210	2-Input OR into 2-Input NAND	5.6×13	16.8×13
XOR20	2-input XOR	9.8×13	28×13
TIE0/1	Tie lo and hi logic	2.8×13	5.6×13
Fill cells	Fill cells for SOC Encounter	Various	Various

Table 5-3. Radiation Hardened Library Input/Output Cells

Cell	Description	Standard Size (μm)	RHBD Size (μm)
BBC1P	1 mA bi-directional pad	95×334	same
BU1P	1 mA output buffer	95×334	same
ICP	Input buffer	95×334	same

5.3.3 Asynchronous Logic Background

Traditional synchronous circuit designs feature a global clock that drives latches surrounding combinational logic, which as a system, performs a particular function. The clock rate is determined by the critical path through the system. This approach has remained an industry standard largely due to the entrenched design flow, which includes design synthesis from HDLs. However, synchronous designs have periodic power peaks, which produce electromagnetic interference (EMI). Additionally, the global clock tree consumes a significant fraction of the required power.

Asynchronous SoC architecture, which offers numerous advantages, has only recently been considered by this niche community [199]. Typically, asynchronous implementations can potentially require a fraction of the power of their clocked counterparts and produce very little EMI. Asynchronous designs are event triggered, processing new data using the minimum number of gate transitions possible. Asynchronous SoC design also promises to solve the global clock

delay problem, which increases as the size of SoCs grow with increased functionality and performance.

Asynchronous logic concepts have existed since the 1950's, offering potential power savings and performance improvements depending on the application [200]. Analogous to RHBD's shortfalls in power and area penalties, asynchronous logic design is more complex when compared to the synchronous commercial standard and carries a potential area penalty. Perhaps the best-reported comparison of power, performance, and area impact of applying asynchronous design to a large commercial circuit, such as the Asynchronous Pentium Front End, can be found in [201]. Recent advances in automating the asynchronous design process have made the idea more attractive, resulting in new commercial offerings.

Asynchronous designs are based on the concept of modular functional blocks with intercommunication using handshaking protocols. The overall function of the circuit resembles that of the synchronous one. Recently, considerable progress has been made to improve the design automation of this particular asynchronous characteristic through *de-synchronisation* [202].

However, de-synchronisation does not yet realize all the potential advantages of asynchronous logic. Although removing the global clock tree and replacing it with a fabric of handshaked interconnections does flatten the power spectrum and reduce EMI generation, it is generally accepted that the opportunity is missed to significantly lower the energy requirements and improve the performance. This can be achieved by recognizing that most synchronous circuits often have redundant operations depending on the system state and that not all operations take the same amount of time. Unfortunately, automating this process has not been achieved due to the variety of power and latency reduction techniques that can be applied, and each one design dependent.

A custom design approach was chosen for this work to demonstrate possible benefits of asynchronous logic, leveraging the assumption that others are continuing to improve asynchronous design automation. The paragraphs that follow describe the general asynchronous design methodologies used in this work. The next section discusses the integration of the RHBD and asynchronous design concepts and presents the comparative results.

A custom design approach was chosen for this work to demonstrate the best possible benefits of asynchronous logic, leveraging the assumption that others are continuing to improve asynchronous design automation. The asynchronous building blocks explored in this effort fall into four categories [203]. The fundamental mode bounded delay methodology is used for blocks with relatively fixed completion times. The delay insensitive design methodology applies to functional blocks with widely varying completion times. Burst mode design methodology applies to components that serve as controllers or asynchronous finite state machines (AFSMs). The

speed independent model specifies the handshaking protocols between major functional blocks. Additionally, ripple-latching and clock-gating are used to further lower EMI and energy use.

The fundamental mode bounded delay methodology is used for functional blocks that have little variation in completion time, such as a latch. This methodology assumes that the delay time through a functional block is known and constant. Worst-case delay, with a margin of safety, is used similar to a clocked circuit. Difficulty arises in synthesizing this structure since timing information cannot be synthesized from behavioural HDL, but can be back-annotated from layout simulations. Figure 5-18 illustrates a delay element used to model the latch completion time. An acknowledge (ACK) signal is asserted when the data is latched after the request (REQ) is generated.

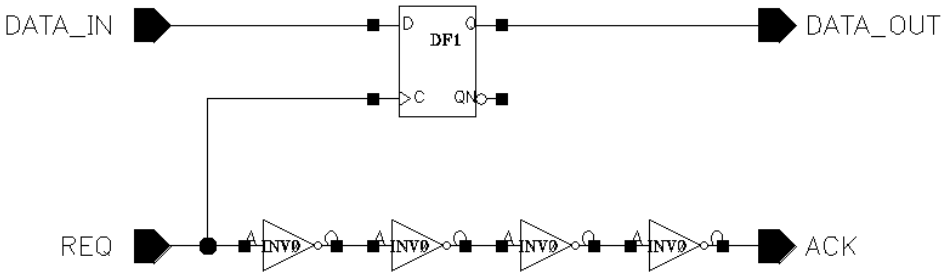

Figure 5-18. Fundamental Mode Bounded Delay Applied to a Latch

A delay element is not suitable for functional blocks with widely varying completion times, since the average critical path latency can be much lower than the synchronous counterpart. Additional logic can be added to this type of block to detect when its execution is complete. Synthesis tools do not yet have the ability to generate the completion detection circuit for a particular functional block, such as a basic add/subtract unit, shown in Figure 5-19.

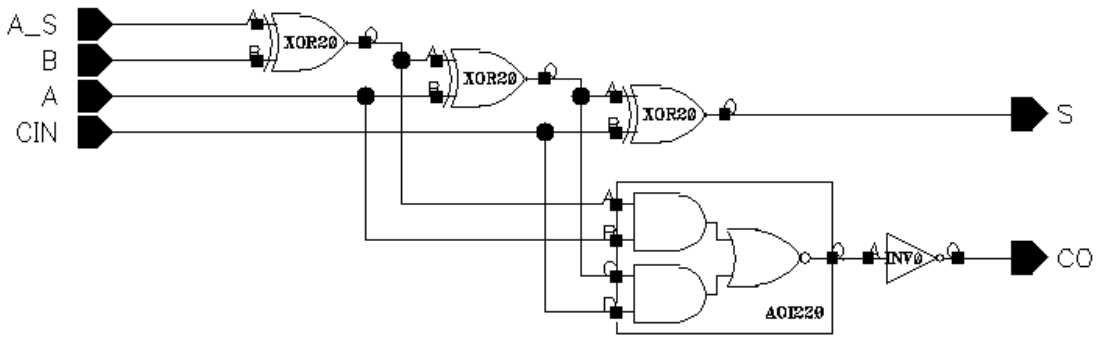

Figure 5-19. One-bit Adder without Completion Detection

A dual-rail adder scheme such as the Manchester propagate, generate, kill (PGK) adder can be used to implement completion detection [204]. The dual rail adder works on the principle that each stage will have either a carry out (COUT) or no carry out (NOCOUT) condition based on the inputs to the stage. Adding 0 and 0 will never result in a carry out, even if there is a carry in. Likewise, adding 1 and 1 will always result in a carry out, even if there is a carry in of 0. Therefore, the carry condition in these cases can be determined by the data to be summed alone and gives early completion detection. Adding a 0 and 1 or 1 and 0 may or may not have a carry out depending on the carry in condition. In this case, the stage must wait for either a carry in (CIN) or no carry in (NOCIN) value. The end result is the completion detection circuit simply becomes the NOR of the COUT and NOCOUT values. Whenever one of these conditions exist, it indicates that all input values necessary for evaluating the sum are present and DONE is asserted. An improved design is shown in Figure 5-20.

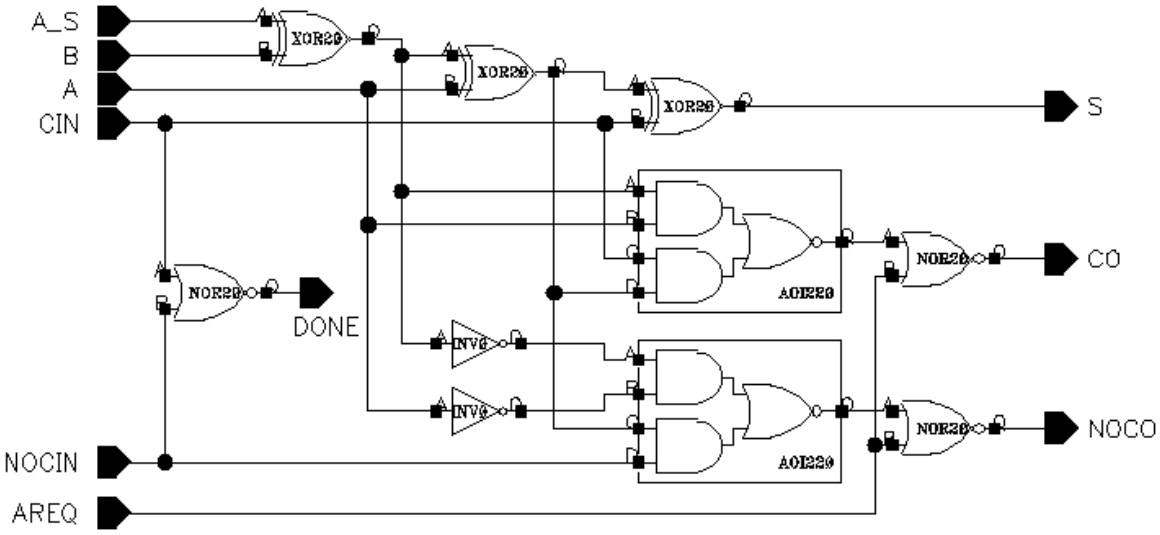

Figure 5-20. One-bit Adder with Completion Detection

The burst mode design methodology is used to design AFSMs. Synchronous finite state machines are easily synthesized by using latches, flip-flops and clock circuitry. Asynchronous controllers or AFSMs must be synthesized using specialized design tools, such as 3D [205].

Functional blocks in an asynchronous design must have a standard handshaking protocol in order to interface with other blocks. A generic functional block in an asynchronous design is shown in Figure 5-21. The REQIN signal represents the external request to the block to input new data. The ACKIN signal is asserted when the new input data is fully latched or accepted. The REQOUT signal represents the request of the functional block to send processed data out. The ACKOUT signal is the external acknowledgement from the next block that the processed data was latched.

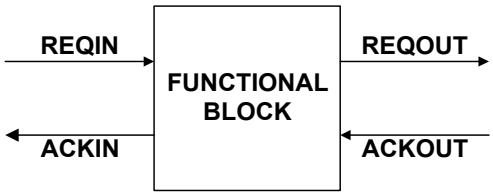

Figure 5-21. Asynchronous Functional Block

The speed independent methodology describes two standards for handshaking between connecting blocks or in this case, the external interface. The four-phase model is illustrated in Figure 5-22. It has a four-cycle handshake for each data exchange.

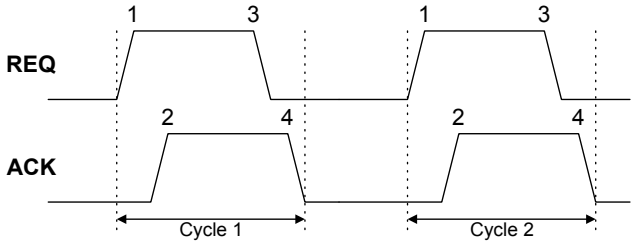

Figure 5-22. Asynchronous Four-phase Handshaking Model

Finally, *clock gating* is a technique developed in the mid-1990's that shares one goal with asynchronous design: to lower the power requirements of a circuit by reducing the amount of switching to an absolute minimum [207]. Clock gating relies on the intelligent application of control logic at various points in the circuit to prevent redundant clocking. The control signal is logically ANDed with the global clock signal to provide a local clock that only switches when necessary. This also allows the use of standard data latches instead of those with an enable circuit. This technique is combined with the unique application of *ripple latching* to flatten the power spectrum and lower EMI.

5.3.4 Case Study of RHBD and Asynchronous Logic Synergy

The basic idea behind this case study was to demonstrate the advantages of using RHBD and asynchronous logic design together. Although area is sacrificed, the aim is that these techniques offer higher performance, a flatter power spectrum, and similar energy consumption when compared to a synchronous design. The combined use of RHBD and asynchronous logic has been previously investigated in [208], greatly expanded upon in [209], with hardware test results in [210]. However, these initial efforts lack a quantitative comparison in simulation and silicon. To make a convincing argument, a common design is selected and implemented in three ways: synchronous with commercial cell library (SC), synchronous with RHBD cell library (SR), and asynchronous with RHBD cell library (AR).

It should be noted that other approaches have been investigated for space applications of asynchronous logic. For example, fault tolerance and deadlock have been addressed by works such as [211]-[213]. These approaches focus on logic gate and circuit level redundancy techniques to improve SEU hardness. However, they exclude TID and SEL considerations, which are mitigated through RHBD. Additionally, asynchronous logic alone has been applied directly in the design of low power wireless sensor nodes [214].

The textbook *MIPS* multi-cycle microprocessor architecture is used as the baseline design as illustrated in Figure 5-23 (adapted from [215]). To keep the size small and affordable, a 16-bit fixed-point 4-register variant (versus 32-bit floating point 32-register) is implemented with a simplified instruction set shown in Table 5-4. The functional block descriptions are given in Table 5-5.

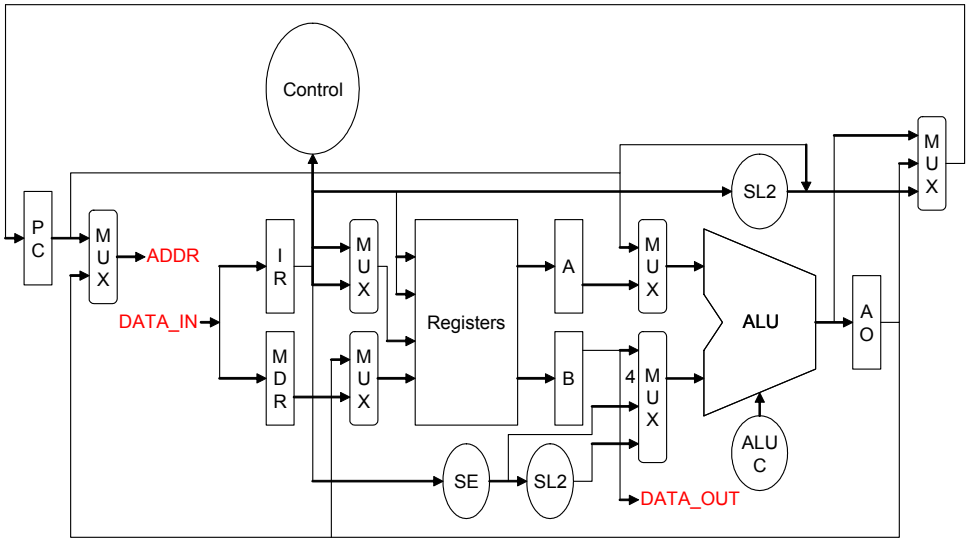

Figure 5-23. MIPS Conceptual Block Diagram

Table 5-4. Simplified MIPS Instruction Set

Instruction	Meaning	16-bit Instruction	Cycles
add	rd = rt + rs	0000rsrtrd000000	4
subtract	rd = rt - rs	0000rsrtrd000010	4
logical AND	rd = rt (bitwise and) rs	0000rsrtrd000100	4
logical OR	rd = rt (bitwise or) rs	0000rsrtrd000101	4
set on less than	set rd = 1 if rt < rs	0000rsrtrd001010	4
load word	rt = mem[rs + addressx]	0001rsrtaddressx	5
store word	mem[rs + addressx] = rt	0010rsrtaddressx	5
branch on equal	if rs = rt go to addressx	0011rsrtaddressx	3
jump	jump to addressx	0100000000000000	3

The entry of the baseline synchronous/commercial (SC) cell design into Cadence is outlined in Table 5-5. The corresponding top-level schematic in Cadence is shown in Figure 5-24. The final layout and micrograph of the SC design is shown in Figure 5-25, as fabricated on AMS S35 run 1725.

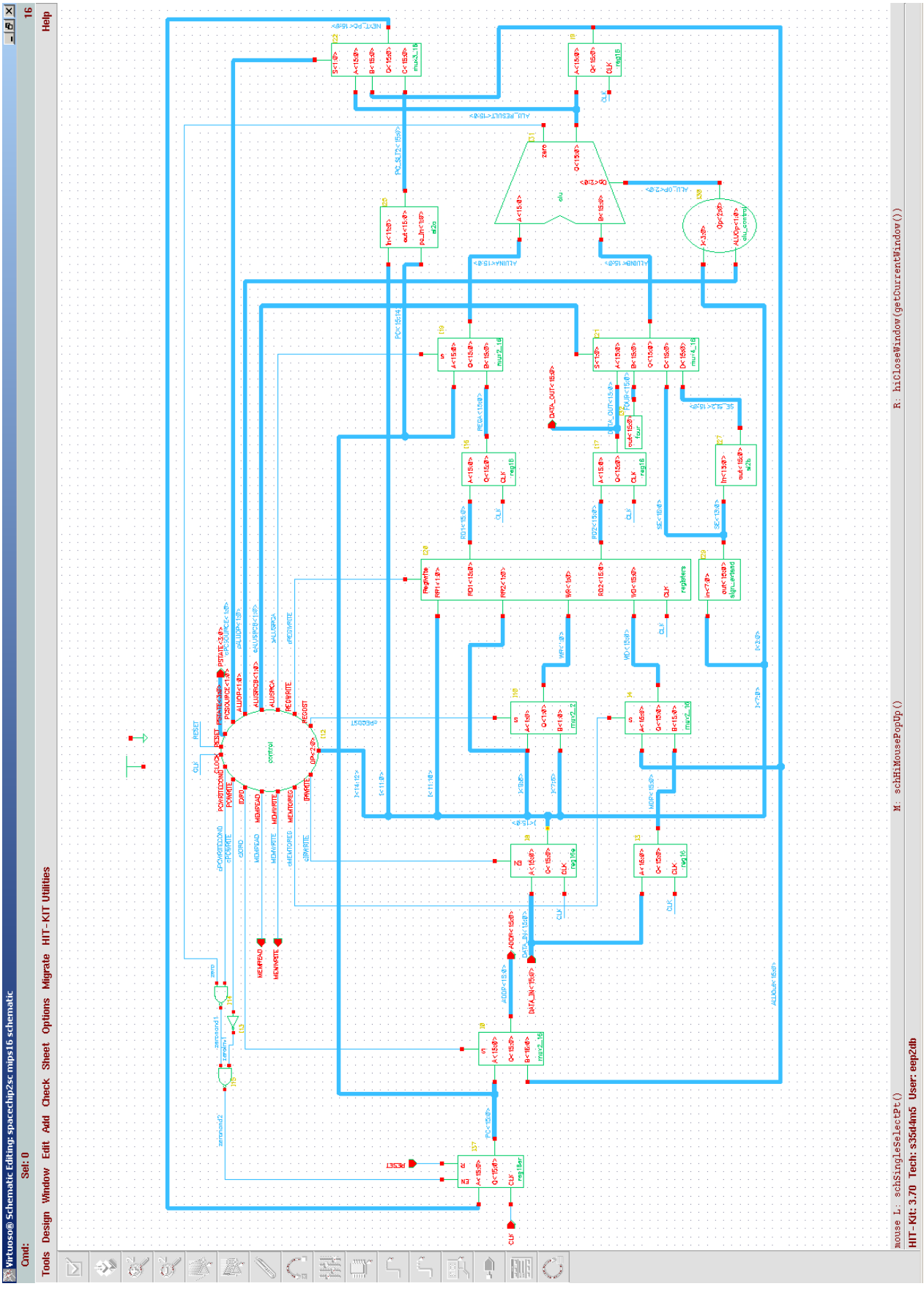

Figure 5-24. Test Chip #2SC MIPS Top-level Schematic

Table 5-5. Cadence Design Flow

Step	Tool	Build Action(s)
1	Library Manager	New design library
2	Virtuoso (Schematic)	16-bit multiplexors (MUX): 2:1, 3:1, 4:1
3	Virtuoso (Schematic)	Arithmetic Logic Unit (ALU) basic block: 1-bit add/sub
4	Virtuoso (Schematic)	16-bit ALU blocks: add/sub, and, or, slt, zero detect
5	Virtuoso (Schematic)	Top-level ALU
6	Virtuoso (Schematic)	ALU control (ALU C)
7	Virtuoso (Schematic)	16-bit registers: Program Counter (PC), Memory Data Register (MDR), Instruction Register (IR), A, B, ALUOut (AO)
8	Virtuoso (Schematic)	Hardwired blocks: Shift Left 2 (SL2), Sign Extend (SE), Four (4), Zero (0)
9	Virtuoso (Schematic)	Top-level register file (3 registers + hardwired 0)
10	RTL Compiler	Synthesis of Control block from Verilog description
11	DFII (Import Verilog)	Import synthesized logic into schematic
12	Virtuoso (Schematic)	Top-level MIPS
13	NC-Verilog	Verilog testbench of all instructions with accurate timing
14	Virtuoso (Schematic)	Top-level chip (adding I/O pads)
15	NC-Verilog	Re-verify testbench, export netlist
16	RTL Compiler	Pass-through of netlist to satisfy SOC Encounter format
17	SOC Encounter	Import netlist, place I/O and core, route, clock tree synthesis (CTS), export netlist, export gdsII stream
18	NC-Verilog	Import layout netlist to schematic, re-verify testbench
19	DFII (Import Stream)	Import gdsII stream to layout
20	Virtuoso (Layout)	Inspect layout and add pin labels
21	Assura	Run DRC, LVS, RCX
22	UltraSim	Run full-chip simulation, compare results with Verilog
23	DFII (Export Stream)	Export gdsII file for fabrication, submit design

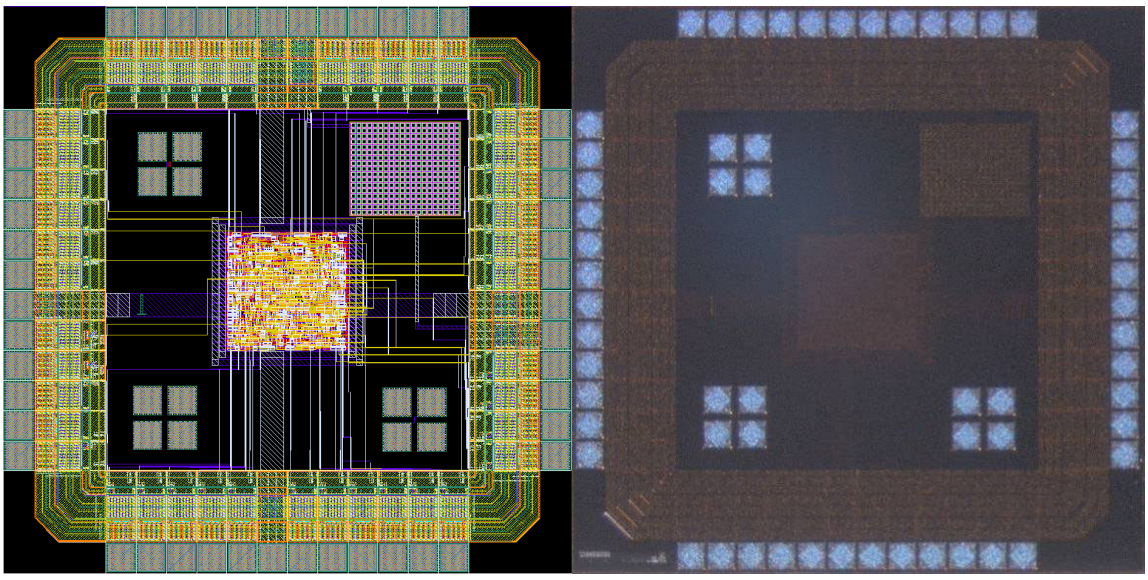

Figure 5-25. Test Chip #2SC Layout (left) and Micrograph (right)

Note the four corner test structures in Figure 5-25. Three of the structures are basic RHBD structures intended for use at a micro probe station: nMOS, pMOS, and an inverter. The fourth test structure is in the upper right hand corner, which is a small bank of photocells with the same initial design structure as Test Chip #1. Test results of these structures are reported in Appendix A as indicated in Table 5-6. These results confirm nominal operation of the RHBD nMOS and pMOS primary cells. The bank of photocells confirms that photocurrent generation in the substrate does not adversely affect the digital circuits nearby.

Table 5-6. Test Chip #2SC nMOS, pMOS, and Inverter Test Results

Test Description	Figure	Page
nMOS Drain Current vs. Drain to Source Voltage	Figure A-1	182
nMOS Linear Voltage Threshold	Figure A-2	182
nMOS Subthreshold Voltage Threshold	Figure A-3	183
nMOS Drain Current vs. Gate to Source Voltage	Figure A-4	183
nMOS Gate Current vs. Gate Voltage	Figure A-5	184
pMOS Drain Current vs. Drain to Source Voltage	Figure A-6	184
pMOS Linear Voltage Threshold	Figure A-7	185
pMOS Subthreshold Voltage Threshold	Figure A-8	185
pMOS Drain Current vs. Gate to Source Voltage	Figure A-9	186
pMOS Gate Current vs. Gate Voltage	Figure A-10	186
Minimum Inverter Operation Voltage	Figure A-11	187

The baseline design is then copied and renamed as the synchronous/RHBD (SR) variant. The SR variant is simply modified by using a global search and replace of the cell library name, beginning at step 14 of Table 5-5. Steps 15-22 are repeated to complete the design. The layout and micrograph of the SR design is shown in Figure 5-26 as fabricated on AMS S35 run 1725.

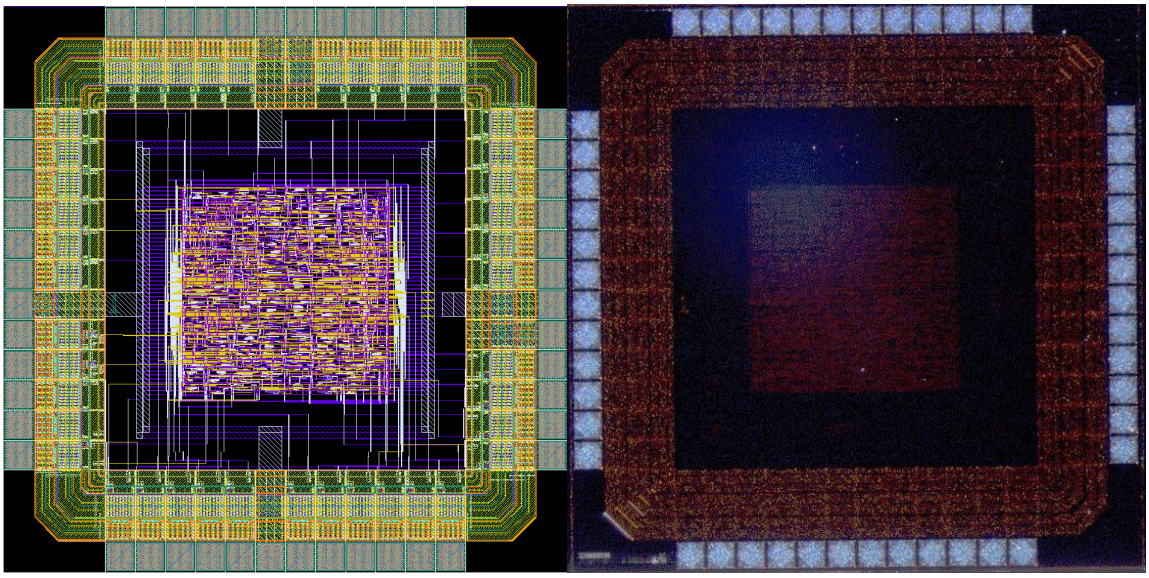

Figure 5-26. Test Chip #2SR Layout (left) and Micrograph (right)

The RHBD library is a layout modification only of the AMS HIT KIT 3.70. The original thought was to use Signal Storm to generate HDL and timing libraries. However, this idea was abandoned due to realizing that this approach would result in reduced drive strength during the various optimisation stages. To maintain radiation hardness to SEU and SET particularly, keeping the drive strength and fanout ratios at the same proportion to the standard cell library is required. Therefore, the best approach is to use the standard cell timing libraries.

There are some minor differences between the two designs just presented, regarding the RHBD cell library. Due to resource constraints, the RHBD library does not have the full array of buffer and inverter cells that are used during clock tree synthesis (CTS). However, the CTS process compensated for this appropriately, as the sum of the transistor widths is the same. In addition, the input/output (I/O) pad cells are the unmodified commercial version, also due to time constraints. This does not affect the simulation or hardware results significantly, as the nMOS transistor widths are equivalent.

The final design in the case study is an asynchronous/RHBD (AR) variant. Asynchronous logic offers potential power savings and performance improvements with a tradeoff in design complexity and usually a small area penalty. In its purest form, this circuit design approach aims to minimise transistor switching. Due to the variety of circuit types and implementation techniques, the design process can be quite complex.

The un-pipelined MIPS architecture may not be the best for demonstrating dramatic power reductions, but it does offer the observer direct insight to the design process. For example, it does not make sense to break down the architecture into smaller blocks where handshaking can be applied. Instead, the MIPS circuit should be thought of as a design block in a larger asynchronous SoC, as in the envisaged architecture of SpaceChip. The external interface of the asynchronous MIPS implementation is shown in Figure 5-21 with four-phase handshaking as in Figure 5-22.

Several asynchronous design methodologies are applied to the synchronous MIPS architecture. This approach is not to be confused with de-synchronisation as defined in [202], but rather a unique focus on overall power reduction and flattening of the power spectrum. The global clock is removed, but instead of replacing the flip-flops with master-slave latches and delay elements as in de-synchronisation, a phased sequence of latching with delay elements (10 buffers in series) is carefully applied across the latches and multiplexers in the data path, as shown in Figure 5-27. Care is taken to ensure a hazard-free sequence and no double-switching of elements. The synchronous FSM control block is improved to minimise latching of the MDR and ALUOut registers. Additionally, a form of clock gating is applied within all registers, which allows the use of basic latches without enables. This also requires latches to be placed on all control signals and phased in as appropriate. The applied approaches are summarized in Table 5-7 and Figure 5-29.

Table 5-7. Asynchronous Design Approaches Implemented

Step	Action	Benefit
1	Remove global clock	Overhead of CTS eliminated, power reduced
2	Add phased latching sequence	Flattens power spectrum
3	Add delays within registers	Further flattens power spectrum
4	Improve MIPS control	Eliminates redundant latching, power reduced
5	Add clock gating	Power reduced
6	Remove unused inverting outputs	Power and area reduced

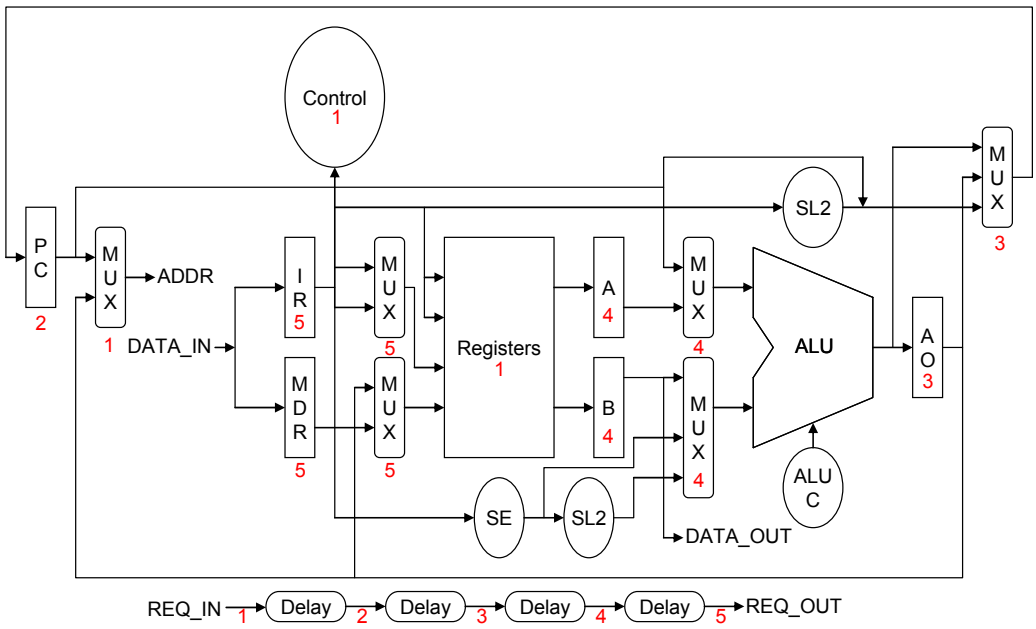

Figure 5-27. Phase-latched Asynchronous Approach

The custom asynchronous adaptation of the MIPS architecture just discussed affects all steps in Table 5-5. Most notable, CTS and optimisation are prevented in step 17. The AR variant was fabricated on AMS S35 run 1791, with the final layout and die micrograph shown in Figure 5-28.

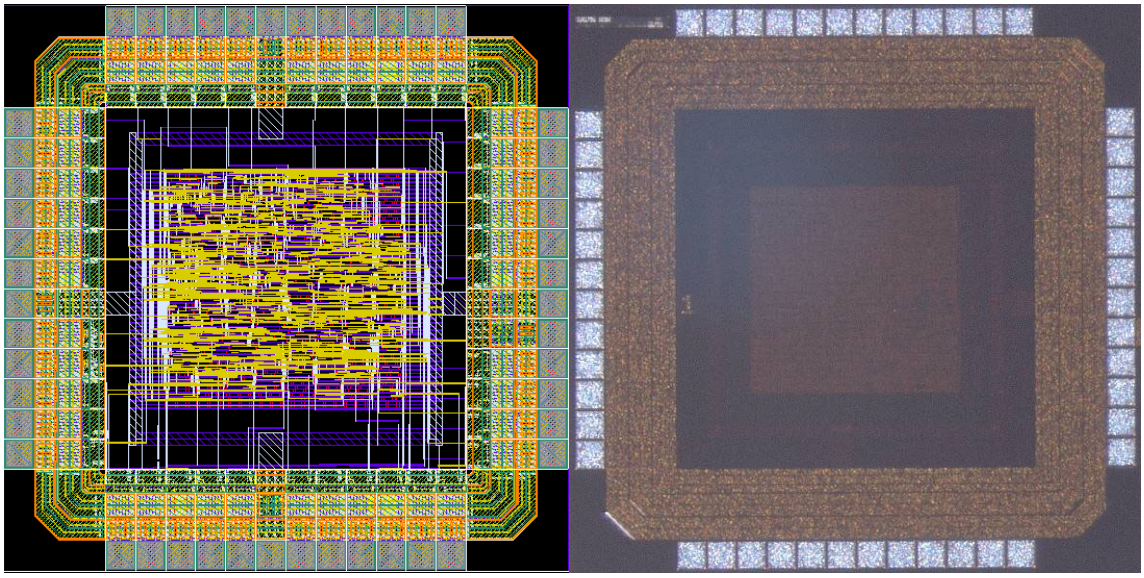

Figure 5-28. Test Chip #2AR Layout (left) and Micrograph (right) Shown with Solar Array

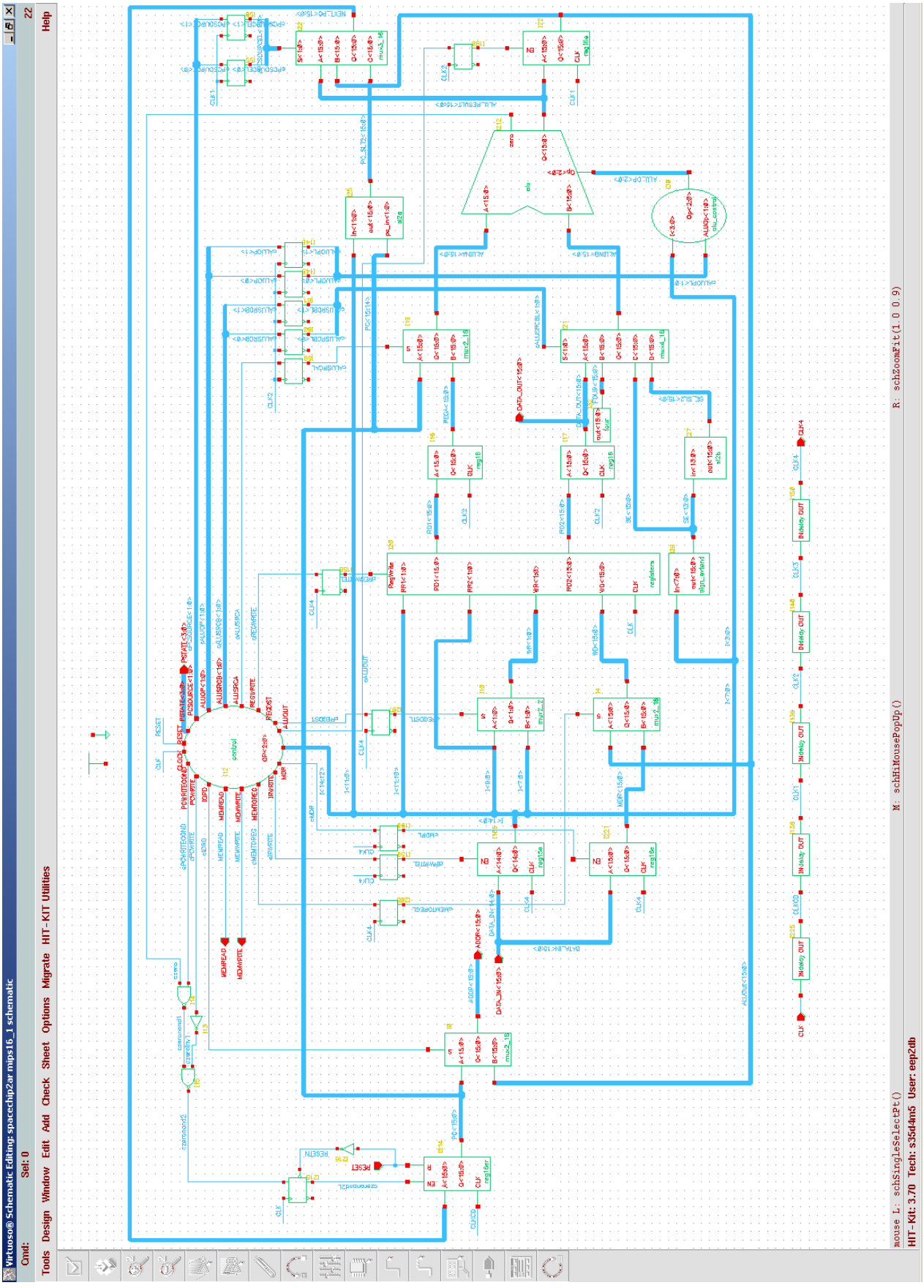

Figure 5-29. Test Chip #2AR MIPS Top-level Schematic

5.3.5 Case Study Comparison, Simulation, and Test Results

A common test bench is used for NC-Verilog simulation, UltraSim simulation, and hardware testing using National Instruments (NI) Digital Waveform Editor and LabVIEW. NC-Verilog is a functional simulator that uses library timing information for each element. Simulation results are available immediately. UltraSim is based on Spice, as it uses extracted parameters for a more accurate simulation, but uses a proprietary algorithm to allow for full-chip simulations in a reasonable amount of time. For example, most of the full-chip simulations require approximately one hour to run, versus hours or days for this size of design on Spice or HSpice. The UltraSim results are advertised to be within 5% of Spice. The test bench is shown in Table 5-8, indicating expected output data (DATA_OUT) and expected address (ADDR) based on the instruction and data mix given to the microcontroller (DATA_IN).

Table 5-8. Common Test Bench Including Expected Results

DATA_IN	Expected DATA_OUT	Expected ADDR
load R1 from address 0x0001		0x0000
0xFFFF		0x0001
load R2 from address 0x0002		0x0004
0x0001		0x0002
R3 = R1 + R2		0x0008
store R3 to address 0x0000	0x0000	0x000C
R3 = R1 - R2		0x0010
store R3 to address 0x0000	0xFFFE	0x0014
R3 = R1 (bitwise and) R2		0x0018
store R3 to address 0x0000	0x0001	0x001C
R3 = R1 (bitwise or) R2		0x0020
store R3 to address 0x0000	0xFFFF	0x0024
R3 = R1 < R2		0x0028
store R3 to address 0x0000	0x0001	0x002C
branch if R1 = R2		0x0030
load R2 from address 0x0002		0x0034
0xFFFF		0x0002
R3 = R1 < R2		0x0038
store R3 to address 0x0000	0x0000	0x003C
branch if R1 = R2		0xFEEC
jump to 0		0xC000

A NI PCIe-6537 50 MHz Digital I/O interface is used for hardware evaluation of the test chips. The I/O interface is mounted in a PCI Express slot of a PC running NI LabVIEW 8.5 and Digital Waveform Editor 3.0. The interface connects to a connector block NI CB-2162 with a NI C68-D4 cable. A zero insertion force socket is used on the connector block with a custom PCB interface to route the socket pin signals to the appropriate connector block pins. A 1.3 ohm resistor is used between the test chip ground and system ground, where a Tektronix TDS 2024 monitors the current draw by measuring the voltage drop across the resistor. The connector block and socket is shown in Figure 5-30 with a test chip mounted.

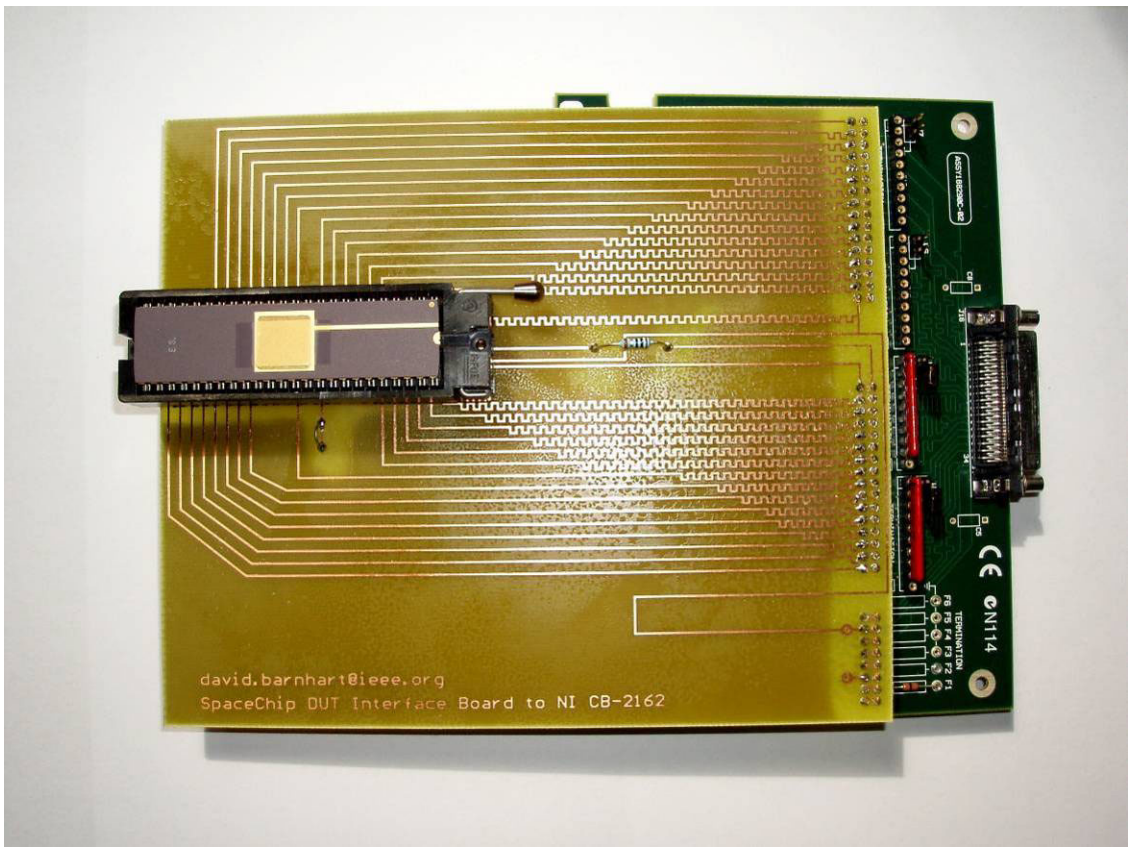

Figure 5-30. Test Chip Hardware Interface

The simulation and corresponding hardware tests results from all designs are shown in Appendix A according to Table 5-9. The maximum frequency of all designs is 16.67 MHz in simulation, but the hardware test platform only operates up to 12.5 MHz. For all three designs, the final hardware functional results at all operating frequencies matches the expected results as determined in NC-Verilog and UltraSim.

Table 5-9. Full Test Chip Results in Appendix C

Description	Figure	Page
Test Chip Pinouts	Table A-1	188
NC Verilog Testbench	Figure A-12	188
UltraSim Testbench	Figure A-13	190
Digital Waveform Editor Testbench and code	Figure A-14	191
2SC NC Verilog Functional	Figure A-16	193
2SC UltraSim and Hardware Functional	Figure A-17	194
2SC UltraSim/Hardware power comparison (full)	Figure A-18	195
2SC UltraSim/Hardware power comparison (single)	Figure A-19	196
2SR NC Verilog Functional	Figure A-20	197
2SR UltraSim and Hardware Functional	Figure A-21	198
2SR UltraSim/Hardware power comparison (full)	Figure A-22	199
2SR UltraSim/Hardware power comparison (single)	Figure A-23	200
2AR NC Verilog Functional	Figure A-24	201
2AR UltraSim and Hardware Functional	Figure A-25	202
2AR UltraSim/Hardware power comparison (full)	Figure A-26	203
2AR UltraSim/Hardware power comparison (single)	Figure A-27	204

Although correct functionality is essential to verify, the most important aspects in this work are the power performance and required core area. NC-Verilog is not able to report on power consumption, so UltraSim is used to compare the design performances before fabricating the devices. A comparison of results is given in Table 5-10. In this case study using a common design, the application of RHBD resulted in a 206% core area increase from the baseline design and required 154% more energy for the same testbench at any frequency, as determined through UltraSim simulations. Figure 5-31 clearly illustrates that all the asynchronous approaches taken to reduce the power and smooth the power spectrum are indeed effective as the power profile is significantly flattened in comparison. The most important result is that the asynchronous approach reduced the energy penalty to 82% (from 154%) for a 6% area increase with no performance impact. An experimental asynchronous version with ALU completion detection requires an additional six nJ in simulation. In all cases, simulations reveal that the I/O pads consume 28% of the reported energy.

Table 5-10. Comparison of Three Design Approaches

Test Chip	Total Transistor Width (μm)	Core Area (μm)	Energy (nJ) (UltraSim)
synchronous/commercial (SC)	16,088	400×400	28
synchronous/RHBD (SR)	60,450	700×700	71
asynchronous/RHBD (AR)	55,973	720×720	51

Figure 5-32 verifies that the final hardware results are correlated with the predicted simulation results, across the 1.25 to 12.5 MHz test points. Each hardware data point is found by averaging the results of ten test bench acquisitions. The most important result is that the asynchronous approach reduced the power by 30% (at fastest clock rate), in both simulation and silicon.

Full test bench and single cycle comparisons of power measurements are shown in Appendix A. In all cases, a significant power increase is seen from the SC to SR case, then dramatically reduced and flattened in the AR case. Additionally, two samples each of the SC and AR test chips are subjected to a brief 100 krad (SiO_2) TID radiation exposure using a Cobalt-60 source, which was the maximum exposure available at the testing facility. As expected, the baseline SC design experienced a dramatic increase in leakage and operational current draw whilst the AR version experienced little change. The complete range of TID and SEE testing would be required to qualify the RHBD library.

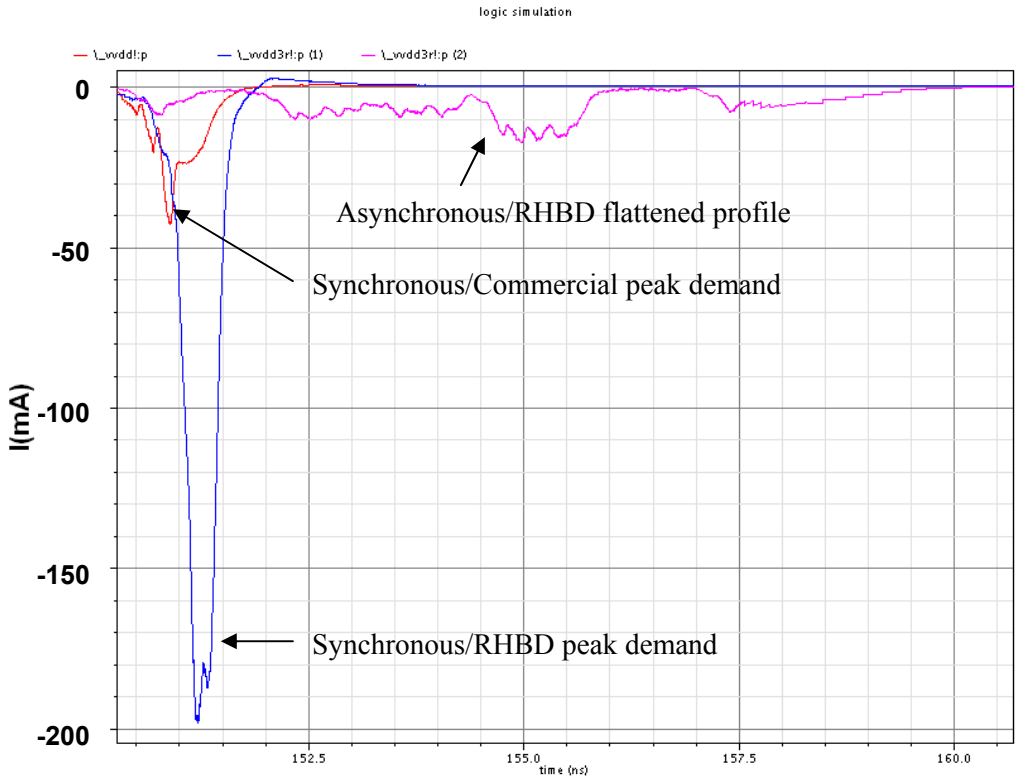

Figure 5-31. Single Clock Cycle Comparison in UltraSim

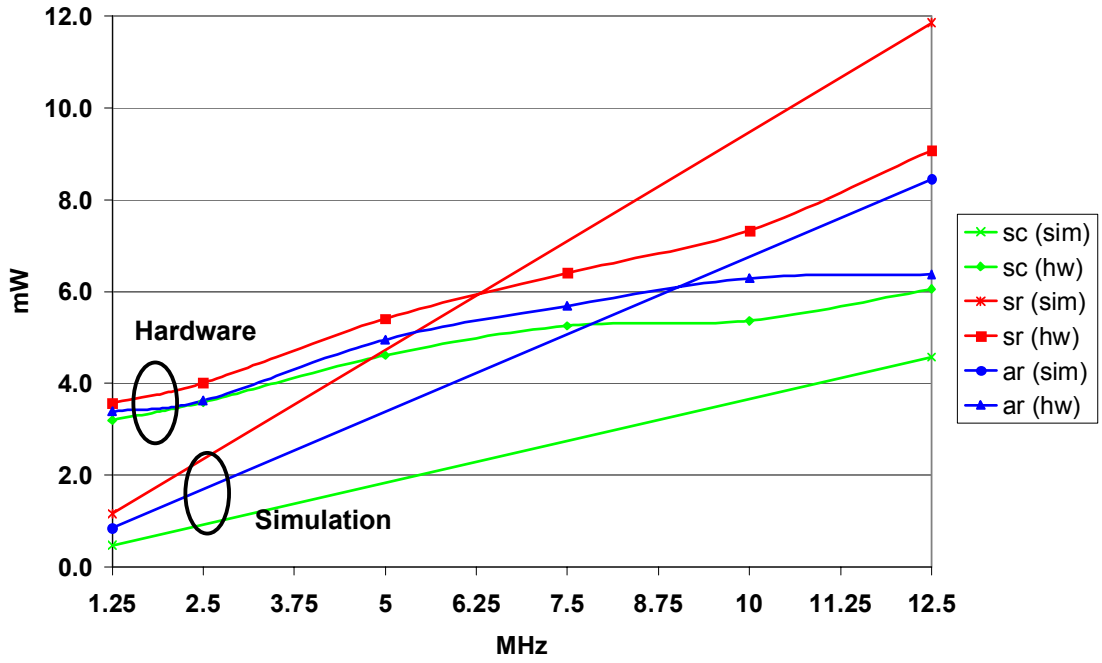

Figure 5-32. Comparison of Simulation and Hardware Power Consumption

5.4 Summary

Heterogeneous SoC sensor nodes are required for wireless sensor network applications in hostile environments. Two essential building blocks to achieve this goal are selected for further development, simulation, and verification in hardware through testing. A technique for monolithically integrating solar cells in SiGe BiCMOS, which can be connected in series to achieve required chip-level operating voltages, is discovered. Secondly, the synergy of radiation hardening by design and asynchronous logic is demonstrated through a convincing case study.

A novel design of integrated solar cells in commercial SiGe BiCMOS is presented. Three prototype designs are designed, fabricated, and tested. The average efficiency of the first prototype is 2.4%, where the actual efficiency of the junction is 8.3%, without considering the metallisation overhead. An improved design demonstrates 3.44% efficiency, a 40% improvement. The junction efficiency alone is 11.3%. A final design that allows for the series connections of cells using a partially insulating layer of the SiGe BiCMOS process yields an efficiency of 2.1%. More research and insight into the process details are required to realize the full functionality of the design. This novel approach has potential widespread application to a rapidly growing number of SoC designs.

Radiation hardening by design and asynchronous logic have been investigated as a complementary solution for bare die system-on-a-chip applications in hostile environments. The synergy of these two design approaches yields a circuit design that can tolerate extremes in radiation, power, process variance, and temperature. A case study using a textbook microprocessor compares the area, power, and performance of baseline synchronous design to design hardened and asynchronous/design hardened variants, all in the same SiGe BiCMOS technology. Radiation hardening by design alone levies a 206% area and 154% energy penalty. The additional application of asynchronous logic reduced the energy penalty to 82% for an additional 6% area with no performance impact. An initial TID radiation screening of 100 krad (SiO_2) revealed the softness of the baseline design whilst the hardened design showed little response.

Chapter 6

6 PCBSat Miniaturisation Approach

PCBSat is a proposed satellite miniaturisation technique focused on determining the smallest practical satellite within the context of space sensor networks. PCBSat, a term coined in this research, began as a conceptual demonstrator for the satellite-on-a-chip concept. Once the practical limitations of satellite-on-a-chip were revealed, PCBSat evolved into a satellite-on-a-PCB approach, which is constrained to using COTS components and deployment systems as discussed in Section 6.1. The derivation of the generic system configuration and structure is then given in Section 6.2. The payload design is presented in Section 6.3. The subsystem designs follow in Sections 6.4 through 6.9, which are geared toward the case study mission, but are intended for application to a range of space sensor networks.

6.1 Introduction

The PCBSat configuration is inspired by the Stensat picosatellite launched in 2000 and discussed in Section 2.3.1.2. Unlike these earlier missions, the focus of PCBSat is to demonstrate satellite commoditisation, where satellites are mass produced with existing infrastructures developed by the personal electronics industry. Low cost leveraging COTS components and practices is essential. At this scale, PCBSat is best suited for massively distributed space sensor network scenarios, versus single-satellite missions, which ideally require at least a CubeSat configuration.

The first prototype design of PCBSat is an attempt to integrate complete, albeit limited, satellite functionality on a single PCB [111] with a mass less than 100 grams. The resulting configuration is shown in Figure 6-1 and Figure 6-2, achieving a mass of 70 grams. Obvious issues arise, such as the space worthiness of such a configuration, as a bare PCB in space will suffer from the thermal and radiation environment. Power is also a concern, both in terms of area available and keeping cells illuminated. As revealed in SpaceChip, a single-sided configuration is unsuitable without robust attitude control, which is an undesirable complication. Secondly, the selected single-chip radio has a range of only a few hundred metres at best and still requires numerous external passives and a supporting PCB area that is many times the size of the chip itself, as seen in Figure 6-1. Nickel-metal-hydride (NiMH) battery technology with its relatively lower energy density proves too bulky at this scale.

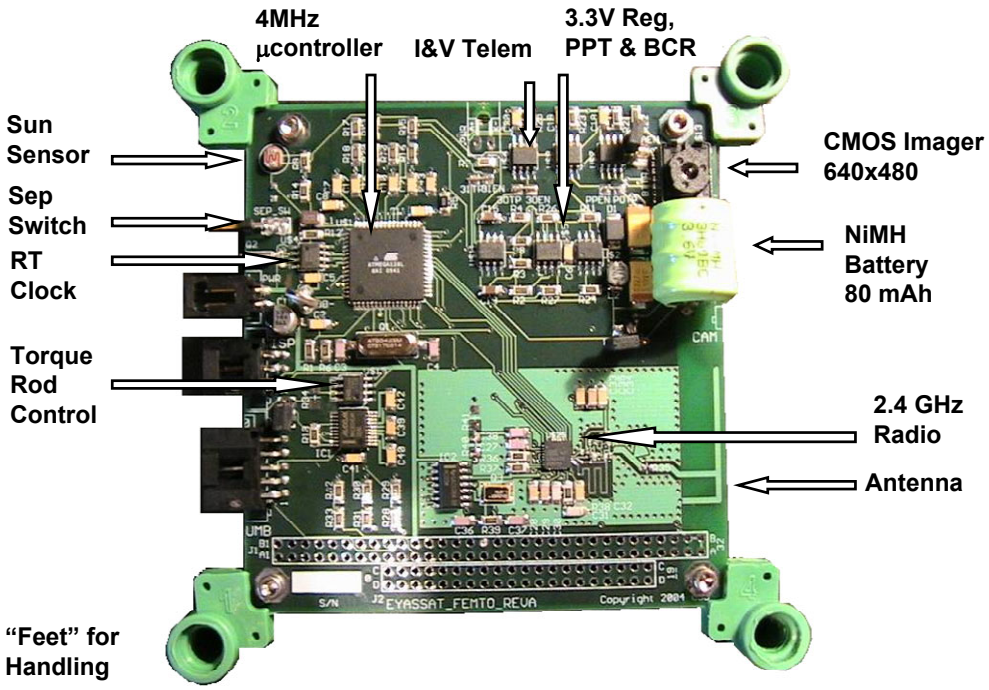

Figure 6-1. Top View of PCBSat Revision A

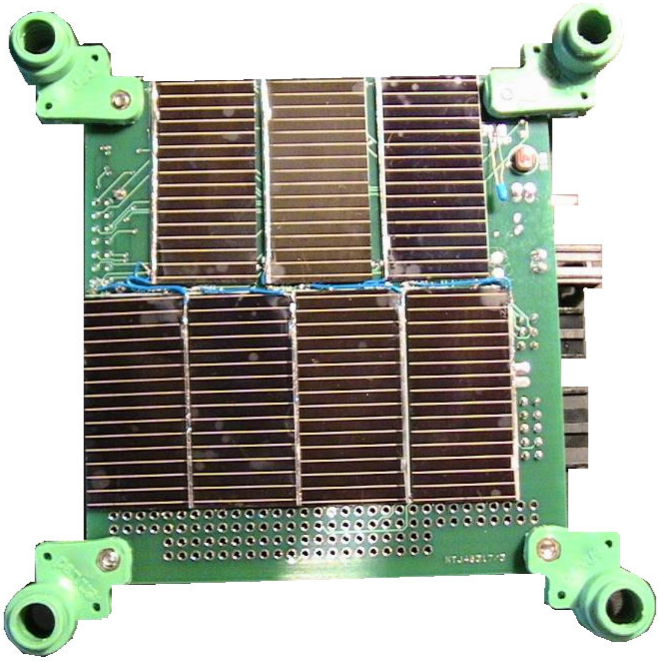

Figure 6-2. Bottom View of PCBSat Revision A

Revisions B and C focus on improving the limited communication range and battery capacity noted in Revision A. Additionally, orbit determination is added, with the integration of a recently developed postage stamp-sized GPS receiver. There are only minor design error differences between revisions B and C. The revised configuration is shown in Figure 6-3. Despite these revelations on the first prototypes, complete EPS and DH subsystem designs are developed, ultimately being used in the final configuration, which is discussed at length in this chapter, including other design issues that arise for each subsystem.

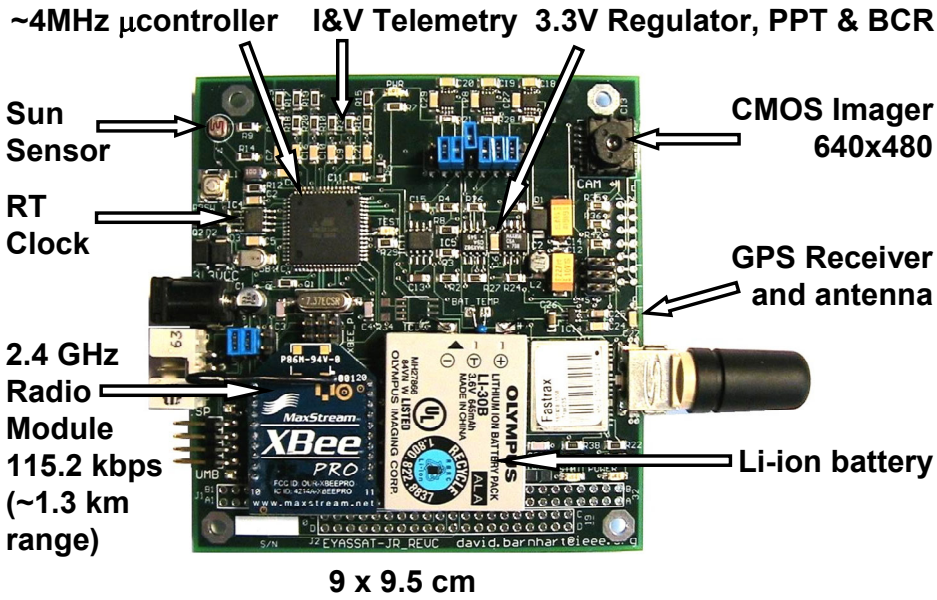

Figure 6-3. Top View of PCBSat Revisions B and C

These early revisions aid the development of the system architecture, but are obviously not aimed at spaceflight. The next section presents the system configuration and structure, which is compatible with the P-POD and X-POD deployment systems. Although generic in nature, the specific implementation illustrated in this chapter is intended to fulfil the requirements of the case study mission presented in Chapter 3.

Similar to SpaceChip, SMAD [11] principles are used throughout the design of PCBSat. At this scale, the design approach is considered *subsystemless* [78], as so many of the components are multifunctional. The PCBSat design is also *bottoms up*, where a finite set of payload and subsystem components, constrained by commercial parts availability, are integrated to determine the overall system capability, which in turn, determines its range of applications. The derived system requirements from the case study mission are shown in Table 6-1. The overall system configuration is shown in Figure 6-4. The derivation of the system configuration is detailed in the remaining sections of this chapter.

Table 6-1. PCBSat System Requirements

System	Requirement	Derived Requirement
Top Level	▪COTS components and manufacturing processes shall be used	▪All but MESA payload
Payload	▪Shall accommodate MESA sensor ▪CMOS imager optional	▪Requires two
Orbit	▪Shall be short-duration LEO suitable for ionospheric plasma depletion study	▪350-500 km, 30-35 degrees ▪5 krad (SiO_2) hardness
Configuration & Structure	▪Shall conform to CubeSat standard and P-POD compatibility	▪10×10 cm (w×l) ▪1 kg/10 cm height
EPS	▪Shall provide power and telemetry through all phases of mission	▪Solar power generation, secondary battery
DH	▪Shall execute mission autonomously or by groundstation command	▪3.3V RISC CPU and FLASH memory, radiation mitigation
Comm	▪Shall demonstrate intersatellite mesh network with 100 km maximum range	▪Co-orbital relay satellite ▪900 MHz ISM, 9600 bps
AOCS	▪Shall position and timestamp data ▪Shall keep MESA ram-facing	▪On-board GPS ▪Passive ADCS
Propulsion	▪None	
Thermal	▪Shall keep all components within thermal limits and provide telemetry	▪Passive

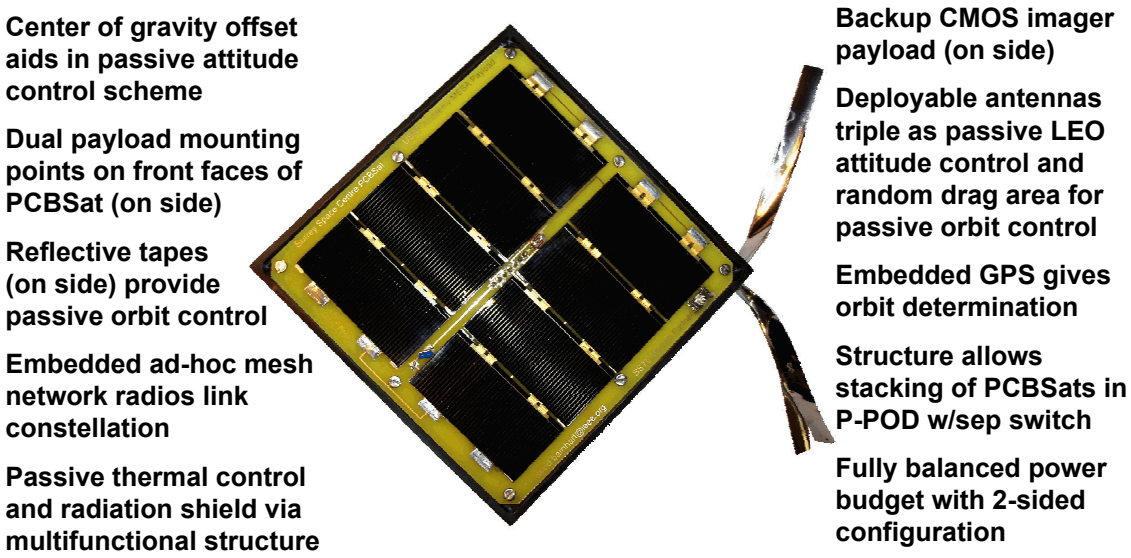

Figure 6-4. PCBSat Flight Model System Configuration

6.2 System Configuration and Structure

The driving system configuration requirement is compatibility with P-POD by conforming to the CubeSat standard summarized in Figure B-1, p. 205 [131]. This fixes the length and width to 10×10 cm whilst the height is a variable, but linked to the mass by P-POD's 1 kg/10 cm thickness

requirement. A minimum thickness of 2.5 cm is a major outcome of this investigation. The P-POD deployer allows up to 8 mm protrusion on the sides of the satellite, between the guide rails. This allowance is used for the mounting of the MESA sensors or any other payload. An exploded conceptual view of the PCBSat system configuration is shown in Figure 6-5.

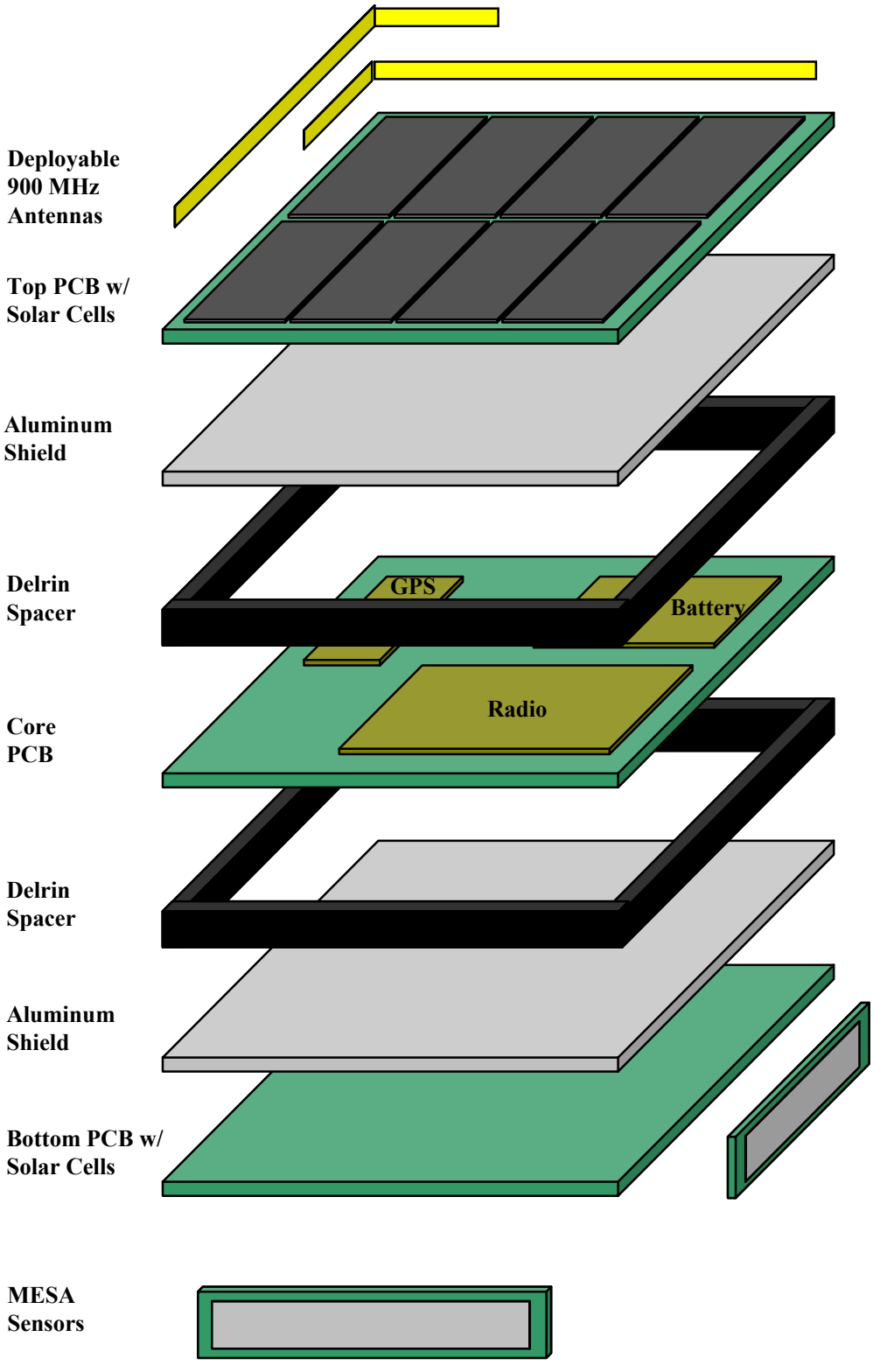

Figure 6-5. Exploded Conceptual View of the PCBSat System Configuration

Ultimately, eight PCBs of differing shapes are required to complete the design, noting the original goal was one. Starting from the top of Figure 6-5, a single-sided PCB is used to mount the solar cells, sun sensor, temperature sensor, and separation switch. Just below this PCB is an aluminium plate, which serves as a passive thermal control, TID radiation shield, and RF ground plane. The core is a two-sided, four-layer PCB, where the topside contains most of the subsystem components, including a battery, radio, and GPS sub-modules. The entire bottom side is devoted to the payload components. All components and ground planes are strategically located to reduce EMI. Mirroring the top, an aluminium plate and solar cell PCB encapsulate the bottom. A two-part space suitable plastic provides the main structural shape, P-POD interface, thermal insulation, and electrical isolation for the two MESA sensor strips and four deployable antennas.

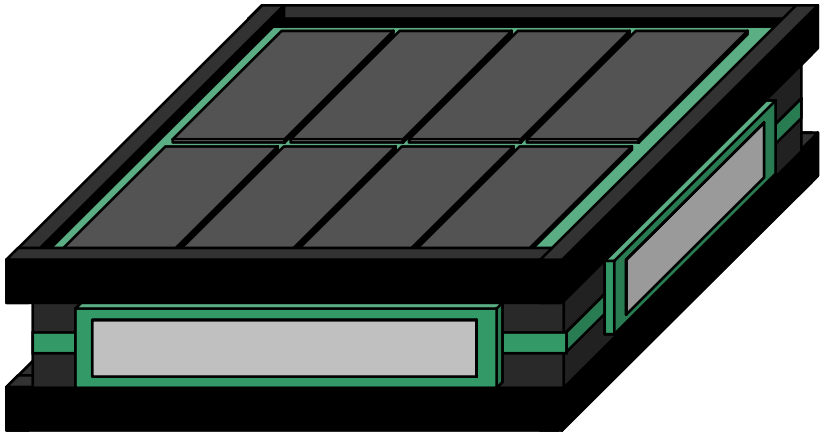

Figure 6-6. Assembled Conceptual View (payload view) of PCBSat

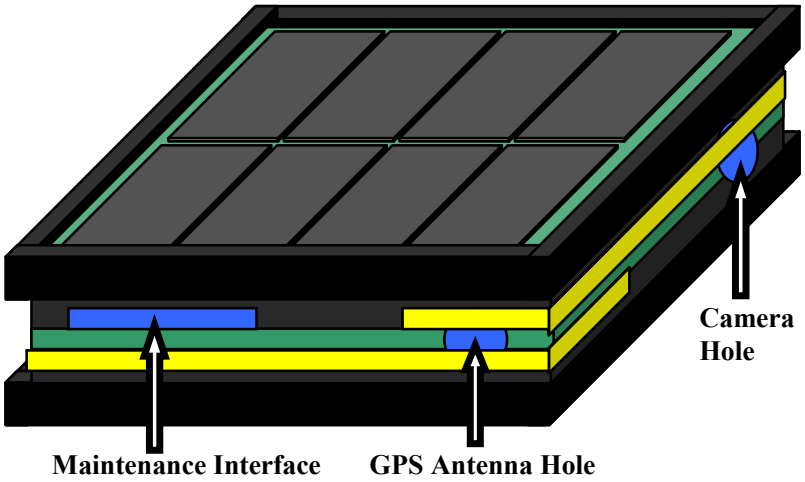

Figure 6-7. Assembled Conceptual View (antenna view) of PCBSat

The core PCB, shown in Figure 6-8, is the most complex assembly in PCBSat, as it integrates the payloads and subsystems. The major components of each subsystem are listed in Table 6-2 and serves as an index to the remainder of the chapter. The two interfaces to the external payload mounting points are on the edges of the PCB, along with an optional CMOS imager, all using right angle headers. The payload interface components are on the PCB underside. The EPS is comprised of two external solar panel PCBs, interfaced by peak power trackers (PPTs) and battery charge regulators (BCRs), which feed the battery and voltage regulator, all telemetered (TLM). The DH subsystem is the heart of the PCB, which interfaces with virtually every payload and subsystem. Comms are provided by a separate module mounted to the core PCB by four standoffs, with the mounting holes clearly seen. The main components of the AOCS are the GPS module and antenna, in addition to the passive attitude control scheme, using a drag tail and centre of gravity (CG) offset. Six thermistors throughout PCBSat comprise the TCS, monitoring the performance of the structural passive control. Finally, a ground support equipment (GSE) interface supports testing, software development, and pre-flight checkouts.

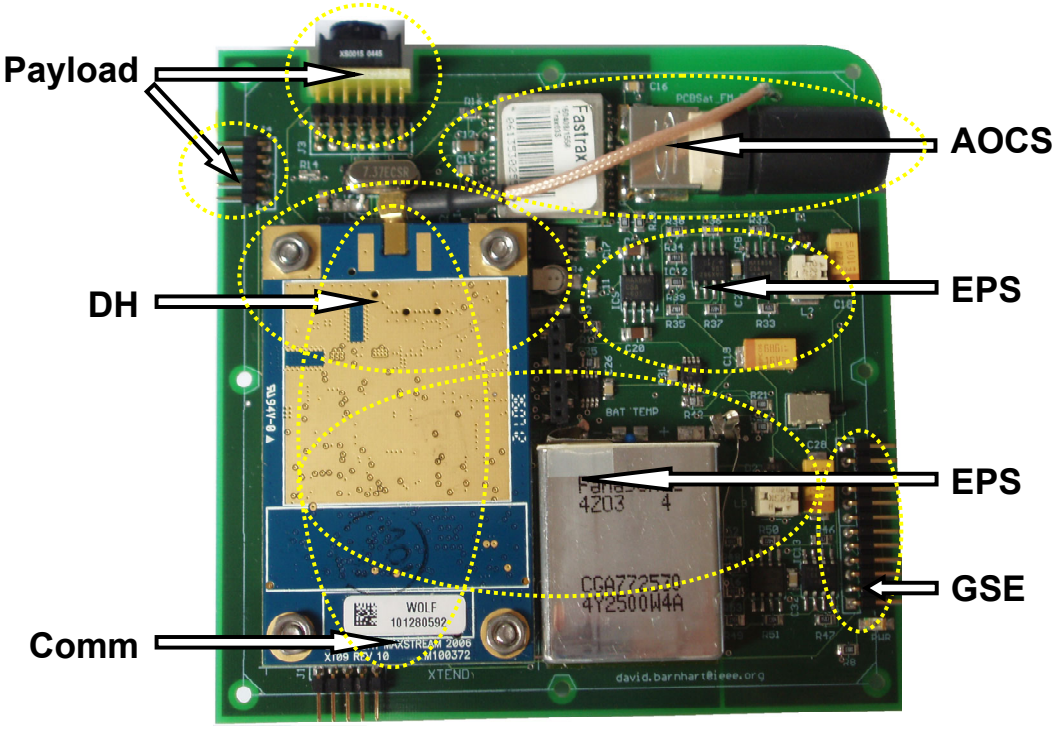

Figure 6-8. PCBSat Core PCB (top)

Table 6-2. PCBSat Major Payload and Subsystem Components

System	Major Components	Section
Payload	MESA1, MESA2, CMOS imager, payload interface (PCB underside)	6.3
EPS	Solar Panel 1 & 2, PPT/BCR 1 & 2, voltage regulator, battery, TLM	6.4
DH	Microcontroller, real-time clock, TLM interface	6.5
Comm	Radio module, deployable antennas	6.6
AOCS	GPS module, antenna, passive control via CG offset and drag tail	6.7
TCS	Six thermistors, passive control via aluminium plates	6.8
GSE	GSE interface to flash programmer, data umbilical, and battery charger	6.9

The spacecraft structure must be designed to protect the payload and subsystems from the forces of launch and the environment of space. The mechanical, chemical, thermal, and electrical properties of all materials must be considered. 6082-T6 aluminium (commonly used in Europe in place of 6061-T6), DuPont Delrin® 107 Black (generically acetal homopolymer), and FR4 PCB comprise the majority of the structural materials used in PCBSat and are commonly used. In terms of outgassing, NASA/ESA typically recommend materials with a total mass loss (%TML) less than 1.0% and collected volatile condensed material (%CVCM) less than 0.1%. UV resistance is also important. Table 6-3 confirms all materials used meet these requirements [11], [216].

Table 6-3. Materials Properties Comparison [11] [216]

Material	Density (ρ) (g/cm^3)	Young's Modulus (E) (GPa)	Yield Stress (σ) (MPa)	%TML	%CVCM
6082-T6-Al	2.70	69	250	-	-
Delrin 107 Black	1.42	3.2	71	0.62	0.01
FR4	1.91	17	-	0.18-0.29	0.01
6061-T6 Al	2.71	69	240	-	-

Regarding the use of COTS electronic components for space, considerations of the material composition, reliability, and environmental tolerance must be made, as summarized in Table 6-4. In general, plastic should be used with great caution. Touching a soldering iron to the plastic component or wire insulation in question is a quick test of its thermal suitability.

Table 6-4. COTS Component Considerations for Spaceflight

▪ Use leaded solder to avoid tin whiskers	▪ Thermoplastic parts should be eliminated
▪ No liquid filled parts (capacitors, batteries, etc.)	▪ Thermosetting plastic parts, including IC packaging, is acceptable but ideally tested
▪ Radiation tolerance (TID and SEE)	▪ Thermal operating range

Finally, the structure design itself must protect the spacecraft during launch by avoiding resonance [217]. However, a structural analysis at this scale is not required if it is solidly constructed and secured using epoxy or locking threads on all fasteners [218]-[219]. A system mass budget is shown in Table 6-5, with a detailed parts list given in Figure B-2, p. 206.

Table 6-5. PCBSat Mass Budget

System	Typical (%)[11]	Typical (g)	Actual (%)	Actual (g)
Structure	22.7	70.5	24.0	74.7
Payload	24.4	75.9	10.7	33.3
EPS	24.6	76.5	29.6	92.1
DH	12.7	39.5	0.6	1.87
Comm			8.8	27.4
AOCS	11.3	35.1	1.2	11.1
TCS	1.7	5.3	22.8	71
Propulsion	2.7	0	0	0
Total	**100**	**311**	**100**	**311**

6.3 Payloads

Numerous miniature payload opportunities exist, as discussed at the chip level in Section 4.3 and at the very small satellite level in [60]. At the PCBSat scale, basic physical constraints still prevent many payloads from being used, such as high-resolution optical systems or high power devices. However, two meaningful payloads are selected for this implementation of PCBSat, supporting the case study mission. The primary payload is MESA, fully described in Section 3.3.4.4. Recall that MESA must be ram facing (i.e. on a spacecraft face normal to the velocity vector) to measure ion activity, but can be in any orientation to measure electrons. To maximize the scientific value of the measurements, both the ion and electron environment is desired, which produces a derived attitude control requirement. A simple passive attitude control technique is used as described in Section 6.7 to keep the MESA sensors on the ram faces. The internal alignment of the plates compensates for the 45° angle. The MESA sensor plates do not have a fixed configuration, as long as the slot size and spacing correspond to the spectrum of interest. Therefore, the planar dimensions of the plates may conform to any available space. For this implementation of PCBSat, an 80×12×8.2 mm configuration is developed for MESA.

As described in Section 3.3.4.4 and illustrated in Figure 3-11, MESA determines the plasma temperature and density by sweeping the voltage on the entrance and exit plates at step intervals whilst measuring the voltage on the collector pad. This is accomplished using a precision digital-to-analogue converter (DAC) to set the voltages on the plates, which are scaled using precision operational amplifiers (op amp). Similarly, the collector plate voltage signal goes through an op amp before it is read by a precision ADC. Both the DAC and ADC are controlled by the system microcontroller (Atmel ATmega128L) through the serial peripheral interface (SPI) bus. This is illustrated in Figure 6-9 and detailed in Figure 6-12.

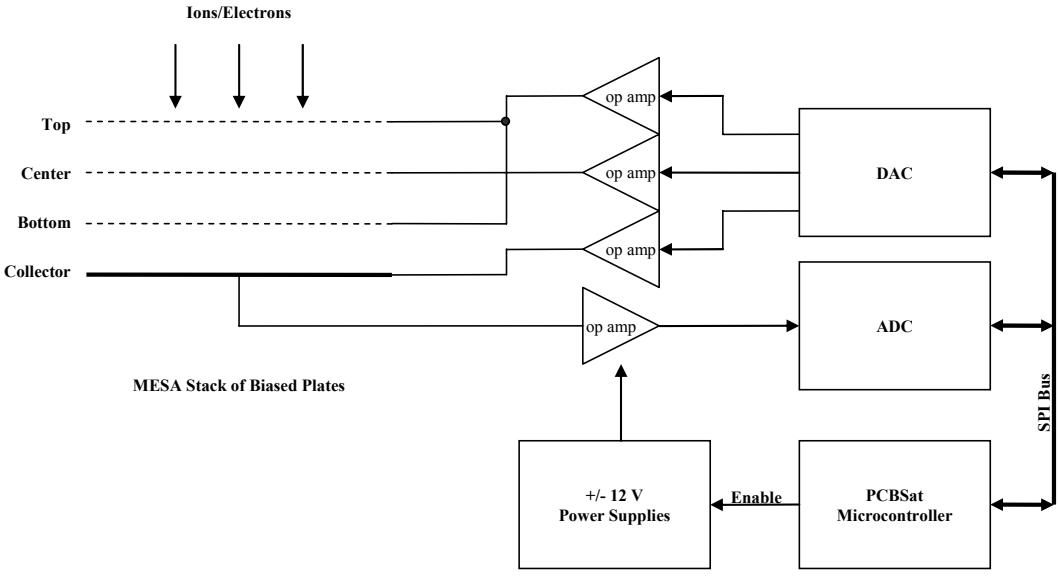

Figure 6-9. MESA Payload Block Diagram

The underside of the core PCB accommodates the payload interface electronics as shown in Figure 6-10, which corresponds to the block diagram in Figure 6-9. An inner-layer digital and analogue ground plane is strategically configured to reduce the EMI generated by the power supplies. The particular use of the MESA payload does not use all the available area. MESA consumes 71.4 mA at 3.3 V (235 mW) whilst operating and can be shut down when required. The PCB layouts are given in Figure B-3 through Figure B-6 starting on p. 208.

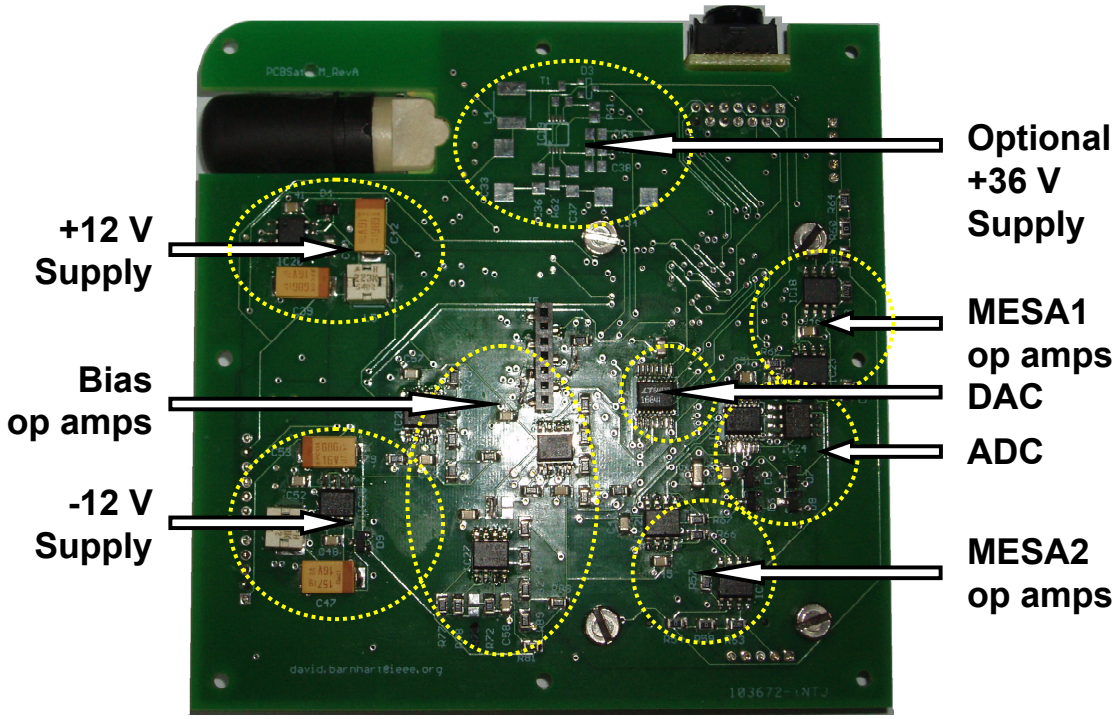

Figure 6-10. Payload Interface Components on the Underside of the Core PCB

Secondly, an ST Microelectronics VS6502 colour CMOS imager with integrated lens is used as a backup payload. Its purpose is to provide low resolution images of constellation deployment and of the Earth. However, no pointing requirements are needed, as pictures will be taken on a random basis. The imager is mounted on the edge of the core PCB and has a viewing hole in the structure. The basic specifications and configuration are shown in Figure 6-11 [220].

- 640×480 pixel resolution, 5.6×5.6 µm pixel size
- Two-wire (I2C) control
- 5-wire data interface
- 2.05 V/lux-s sensitivity
- +37 dB signal/noise ratio
- 2.6 to 3.6V supply voltage
- <30 mA current draw in video mode
- 0 to 40 °C operating temperature
- 11x9x6 mm package size, 14 pad SmOP package
- 47° field of view, f#2.8

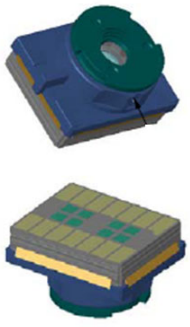

Figure 6-11. ST VS6502 CMOS Imager [220]

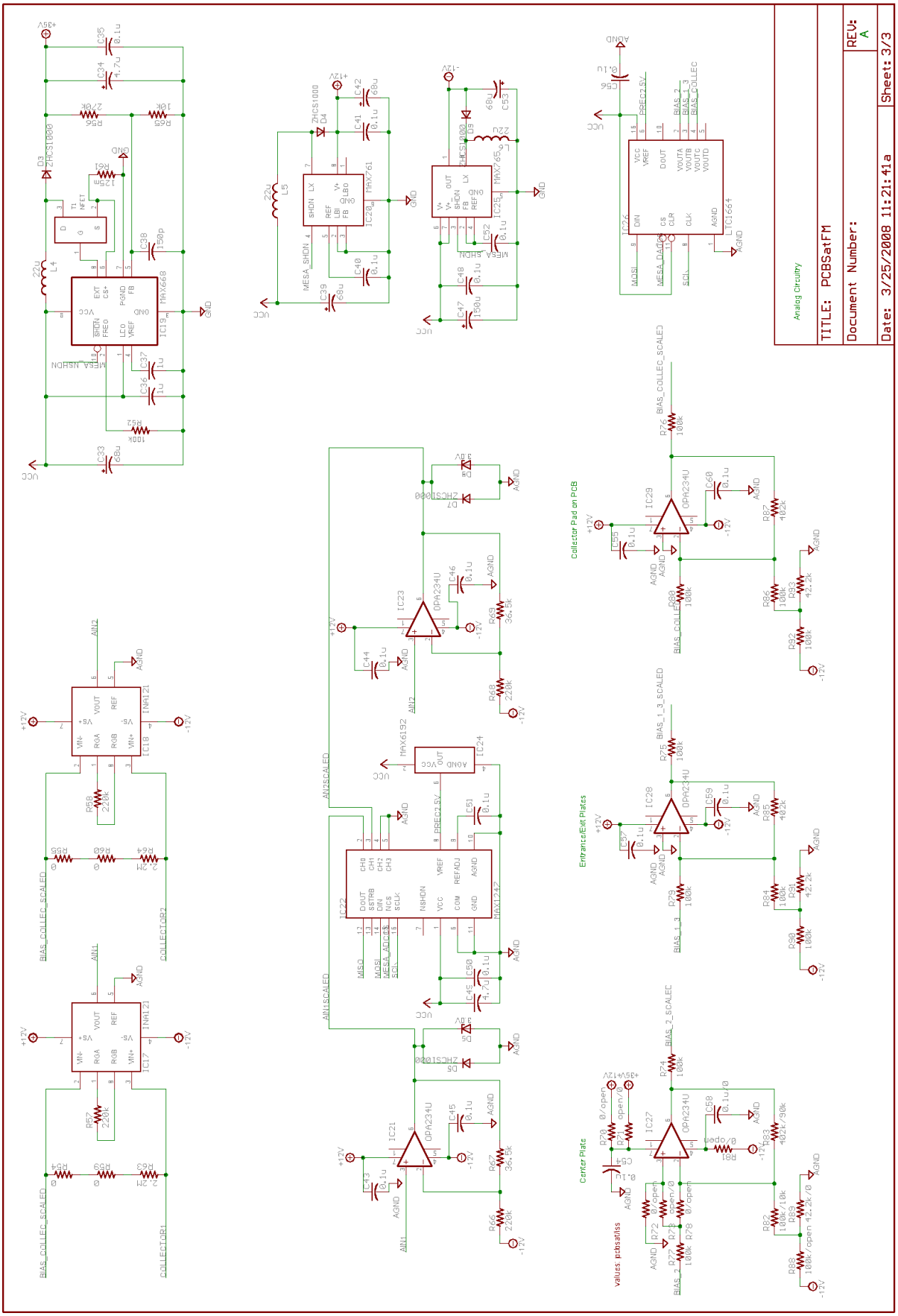

Figure 6-12. PCBSat MESA Schematic

6.4 Electrical Power Subsystem

A power budget is developed as shown in Table 6-6 for PCBSat with the MESA payload. Recalling the nature of ionospheric plasma depletions, the phenomenon only occurs between dusk and dawn, which corresponds to orbital eclipse. Therefore, MESA and GPS (for time and location stamping) will only need to operate during this time. This gives a sunlit power requirement of 381 mW and an eclipse power requirement of 353 mW. The details for each subsystem shown are discussed in the corresponding subsystem sections to follow, using all measured values reported in Table 7-1, p. 128.

Table 6-6. PCBSat Power Budget

System	Typ. (%)	Max (mW)	Sunlit Duty Cycle (%)	Sunlit Power Req't (mW)	Eclipse Duty Cycle (%)	Eclipse Power Req't (mW)
Payload	40	235	0	0	100	235
EPS	20	X_s/X_e	-	-	-	-
DH	10	18	100	18	100	18
Comm RX	30	264	100	264	0	0
Comm TX		1980	5	99	0	0
AOCS	0	100	0	0	100	100
Propulsion	0	0	-	-	-	-
Thermal	0	0	-	-	-	-
Structure	0	0	-	-	-	-
Total	100%	2597 mW	**-**	**381 mW**	**-**	**353 mW**

As determined in Section 4.4, a 500 km circular orbit gives a period P of 94.6 minutes, a sunlit time T_s of 58.9 minutes, and an eclipse time T_e of 35.7 minutes. The required solar array power for PCBSat is found to be 857 mW using Equation 4.5, results from Table 6-6 (P_s = 381 mW, P_e = 353 mW), a measured sunlit power transfer efficiency X_s of 76%, and an estimated eclipse power transfer efficiency X_e of 60%.

The 857 mW power output is the required average output from the solar array. Considering that PCBSat is not sun tracking with only passive attitude control for MESA, the average incidence angle to the sun must be estimated. A conservative estimation is to consider PCBSat to be a very thin CubeSat, where there are twice as many faces without solar cells than ones with cells [221]. Therefore, the average angle of the sun to a face with cells is *(cos 45)(cos 45)* = 0.5. This implies that the 857 mW requirement must be doubled to determine the minimum solar array output, which is 1714 mW. Meeting this requirement is a careful balance of cost versus performance, as power generation at this scale turns out to be one of the most important metrics when comparing very small satellites as discussed in Chapter 8.

The first PCBSat prototypes use hobby-grade ($5 each) silicon solar cells with an advertised 11.4% efficiency at AM0 conditions (1366 W/m^2). A maximum of seven 2×4 cm cells can be placed on the prototype PCB due to though-hole components on the edges of the 96×90 mm PCB. The resulting performance of the 56 cm^2 array is shown in Figure 6-13, where 484 mW are generated, resulting in an actual efficiency of 6.3%, averaged over three different array measurements. Halving this number to account for the average incidence angle gives 242 mW, which is far below the required value.

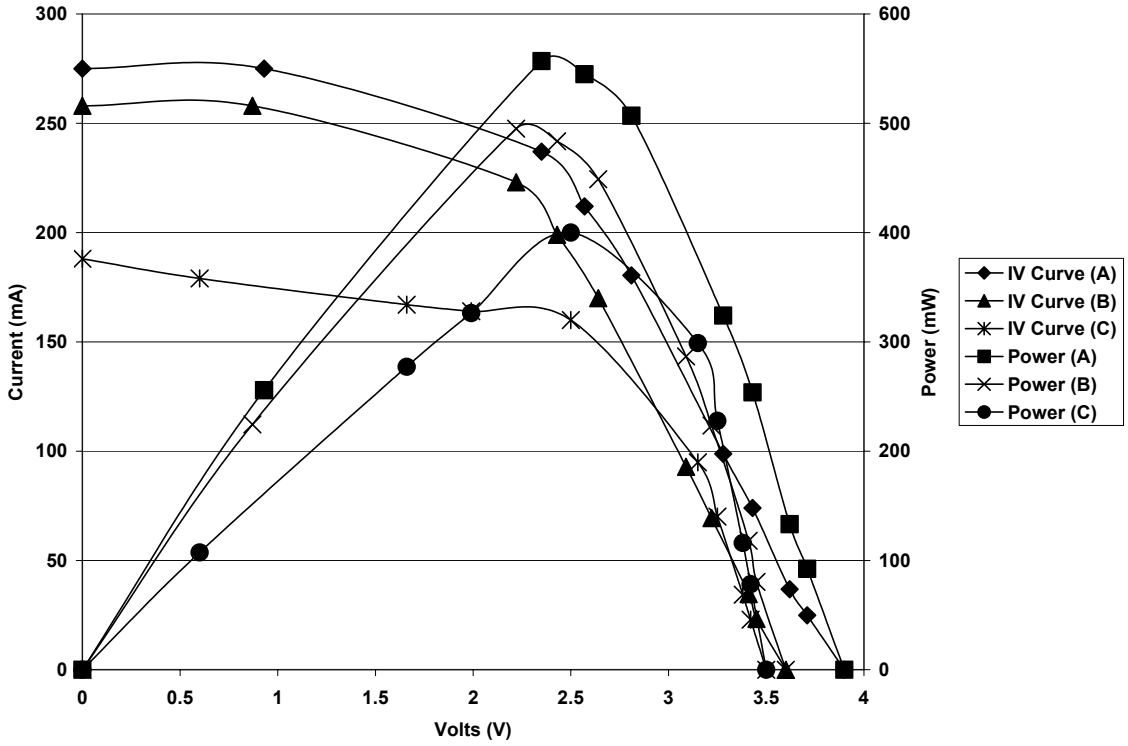

Figure 6-13. Hobby Cell Grade Silicon Solar Array Data Performance, AM0

Two solar cell configurations are possible. Single-junction 2×4 cm GaAs/Ge cells are 18% efficient at 860 mV, 25°C, AM0 [222]. With two parallel strings of four cells in series for redundancy, this translates to 1574 mW or 457 mA at a peak point of 3.44 V. Halving this result yields 787 mW on average, falling short of the 857 mW requirement by 10%. Surprisingly, a less expensive option is two triple-junction, 6.9×3.9 cells, providing 1760 mW or 880 mW on average, which meets the 857 mW requirement. The triple-junction cell cost is used in the cost modelling given in Chapter 8. Solar environment test results are reported on in Section 7.2.2.

The second most important EPS parameter is the battery capacity. The total required capacity of the battery C_r is found using Table 6-6 and Equation 6.1. The total required capacity of 291 mAh assumes an 80% depth of discharge (DOD) for a four-month mission and a 90% transmission efficiency n between the battery and the load, which are both typical values.

$$C_r = \frac{P_e T_e}{(DOD)n} = 291\ mAh \tag{6.1}$$

Finding a battery with this capacity is not difficult, but meeting the form factor and mass requirements is challenging. A 3.6 V Panasonic CGA772530 lithium-ion (Li-ion) prismatic battery with a 645 mAh capacity is used. It measures 30×25×8 mm, 13 grams, is encased in aluminium, and costs only 50 cents. Figure 6-14 [223] illustrates that keeping the battery warm is essential. Figure 6-15 [223] reveals the known and rapid capacity loss of Li-ion technology due to cycling. However, on-orbit results should be better, as the eclipse current draw is only 107 mA.

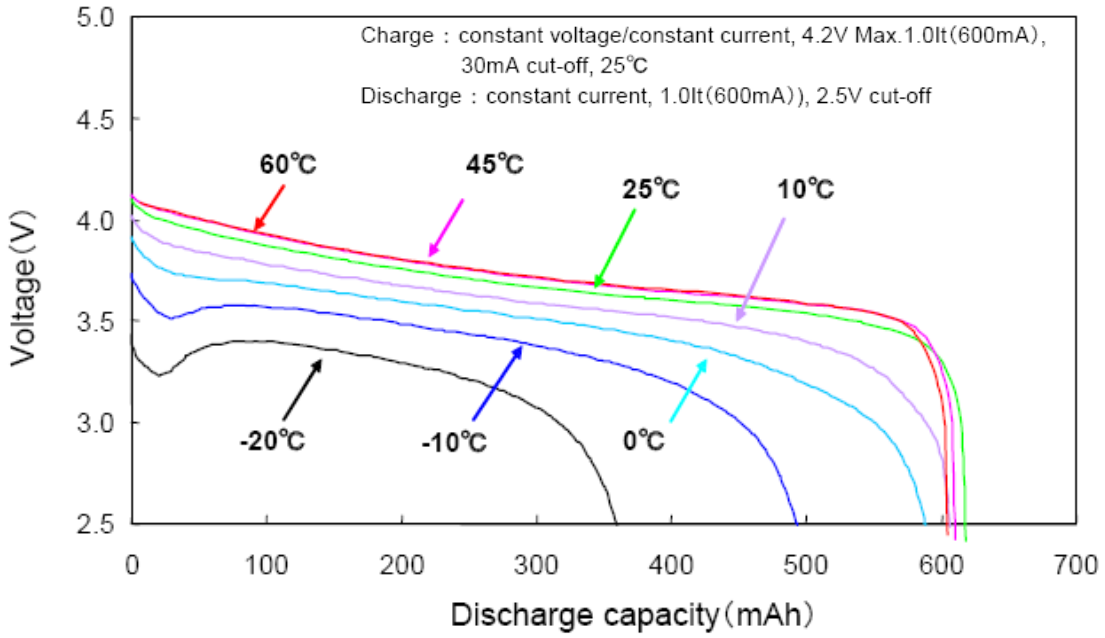

Figure 6-14. Panasonic CGA772530 Capacity vs. Temperature [223]

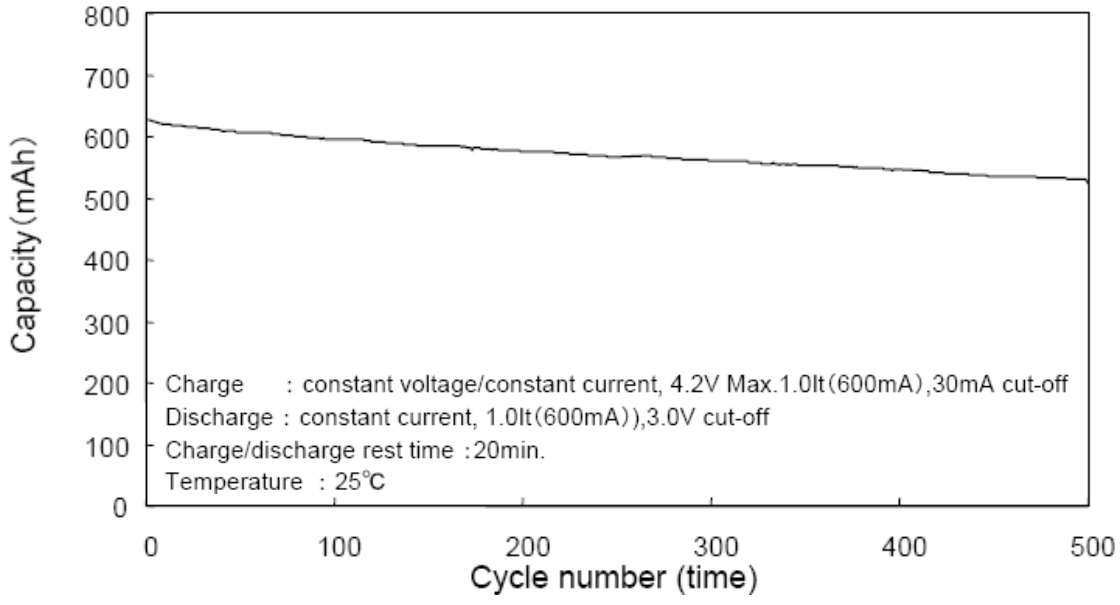

Figure 6-15. Panasonic CGA772530 Capacity vs. Cycles [223]

With the solar array and battery defined, the remainder of the EPS is designed, which consists of two PPTs, two BCRs, a 3.3 V voltage regulator, and eight points of telemetry. The PPT and BCR is based on an example application circuit from Maxim Integrated Circuits (MAX) as shown in Figure 6-16 [224].

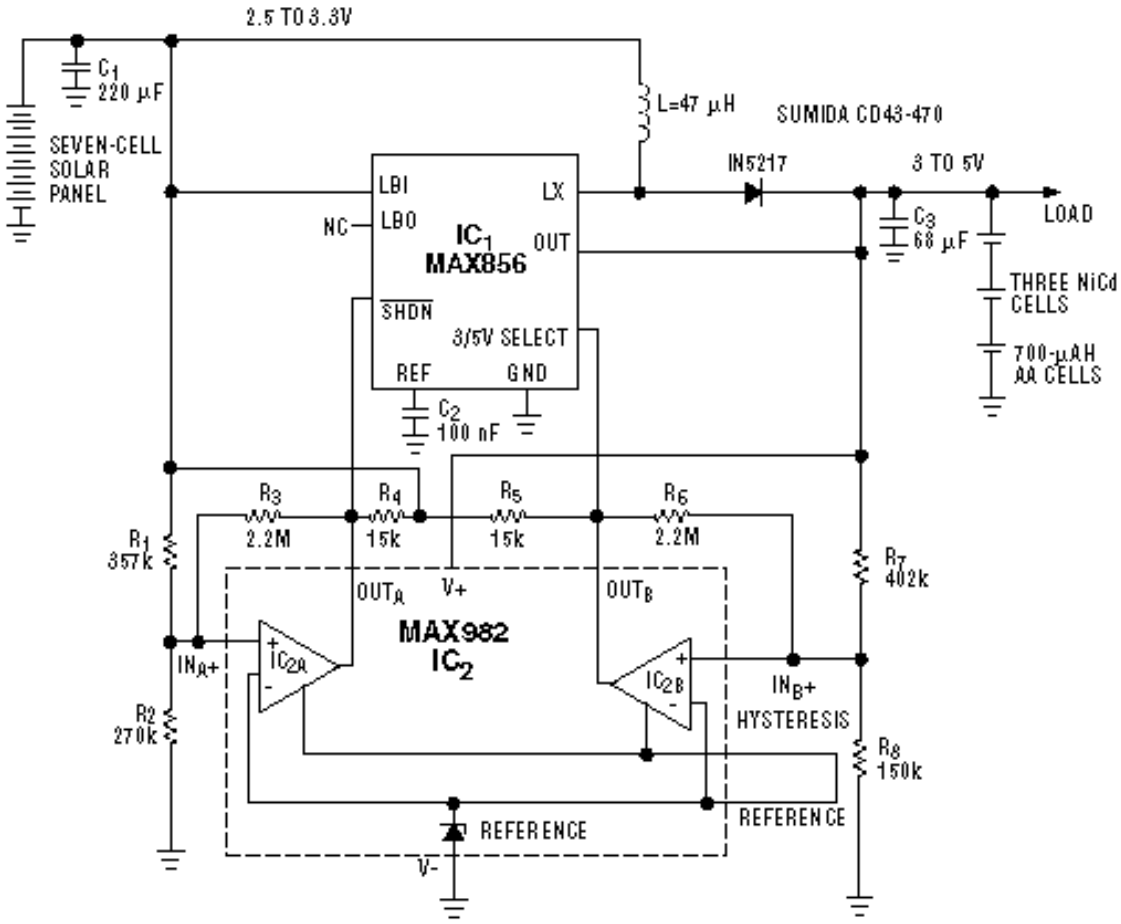

Figure 6-16. Example PPT/BCR Circuit [224]

The operating principle of the PPT portion of the circuit is straightforward. C1 accumulates the charge from the solar array. When the voltage on INA+ of the MAX982 voltage comparator matches the pre-set peak power point of the array (set at 3.44V with R1 and R2), the MAX856 DC-DC converter is activated at 5 V until the solar array voltage drops below 3.44 V, with a small hysteresis. The BCR side of the circuit monitors the voltage on the battery, which is measured at INB+. When the battery voltage exceeds the threshold (4.4 V set by R7 and R8), the MAX856 is set to output 3.3 V, which in effect does not charge the battery, but instead bleeds the power off internally. The measured end-to-end PPT/BCR efficiency is 82.7%, as used in Equation 5.3.

The battery is protected from overcharging by the BCR and from excessive current draw using a self-resetting poly switch. It is disabled whilst awaiting launch in the P-POD using a remove before flight (RBF) switch. The battery is then connected to a MAX604 3.3 V linear regulator,

which is 92% efficient, when stepping down from 3.6 V to 3.3 V. Eight points of current and voltage telemetry are accomplished by MAX4072 bidirectional current sense devices and voltage dividers that monitor both solar cells, the battery, and system 3.3 V. These analogue readings are measured by the ADC inputs of the ATmega128 microcontroller, discussed in the next section. A MAX4634 analogue multiplexor is used, as there are only eight ADC inputs available, which are shared with the thermal sensors. The EPS block diagram is shown in Figure 6-17 with the complete schematic given in Figure 6-19. The solar array PCBs are shown in Figure 6-18.

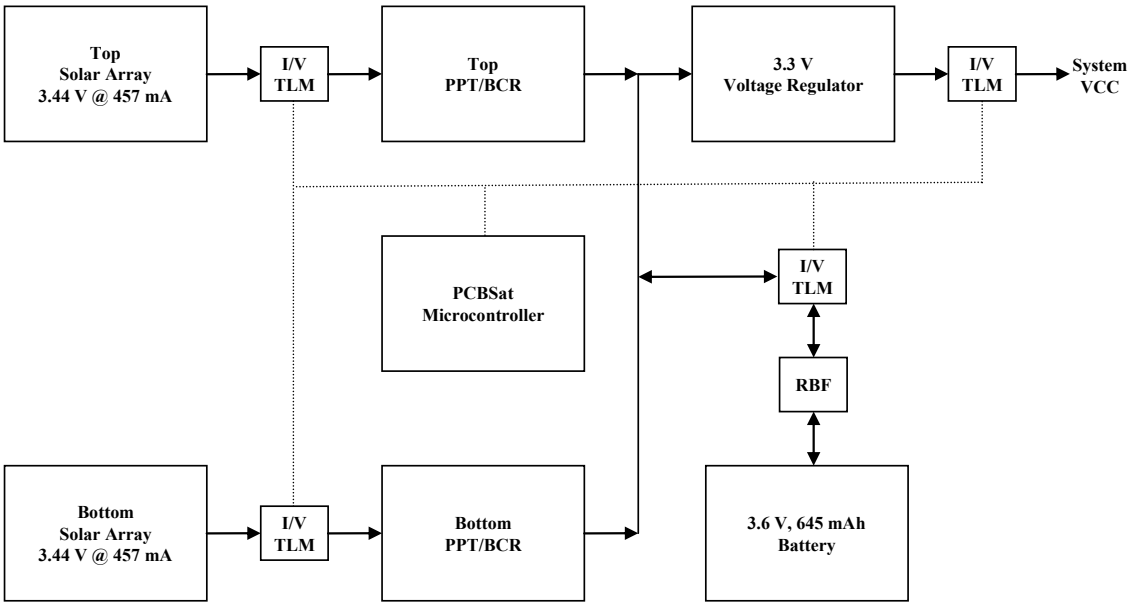

Figure 6-17. EPS Block Diagram

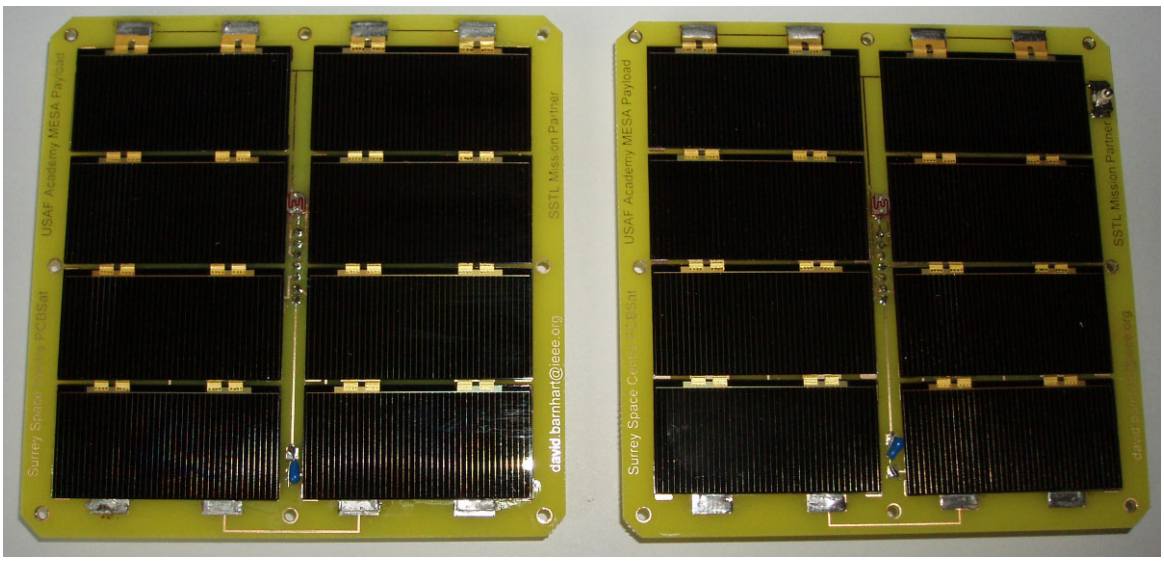

Figure 6-18. EPS Solar Array PCBs

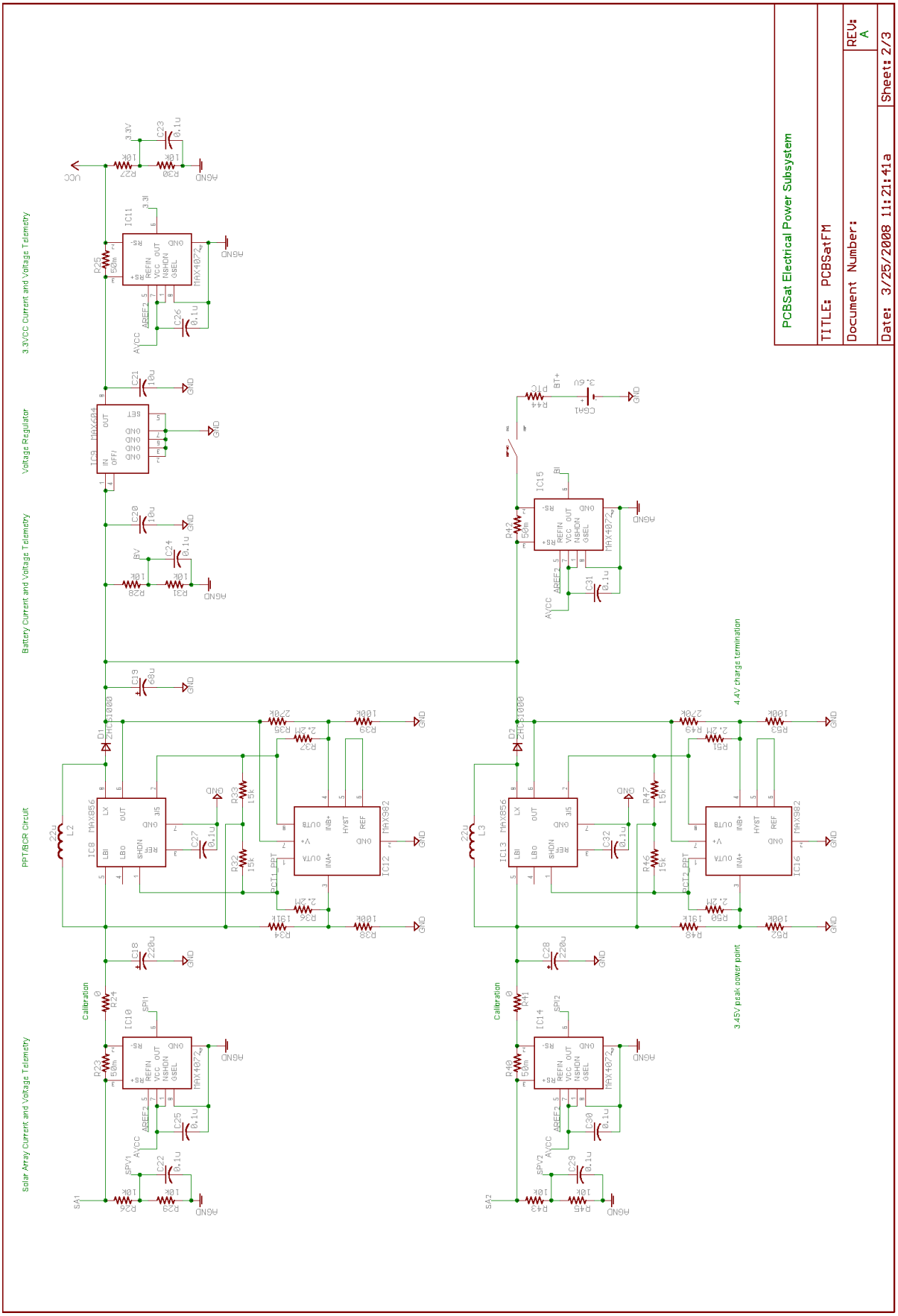

Figure 6-19. PCBSat EPS Schematic

6.5 Data Handling Subsystem and Firmware

The chosen core of the DH subsystem is the Atmel ATmega128L 8-bit AVR® low-power microcontroller. It is ISP programmable via a 6-wire AVRISP® programming interface to a PC. It also has a boot loader option, which is essential for updating software once deployed. CodeVisionAVR is used as the software development environment. The basic specifications are given in Figure 6-20 [225].

- Low-power 3.3V variant
- 8 mA draw at 8 MHz clock
- ISP/boot-loader programmable
- 128K flash memory
- 4K EEPROM
- 4K SRAM
- Four counters
- 8-channel 10-bit ADC
- Dual USART interface
- SPI data interface
- I2C data interfaces
- 53 multipurpose I/O lines

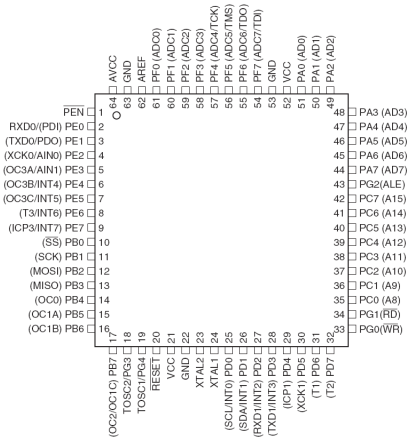

Figure 6-20. Atmel ATmega128 8-bit AVR® Microcontroller [225]

The DH subsystem block diagram is shown in Figure 6-21 with the detailed schematic in Figure 6-23 at the end of this section. The ATmega128L's 128K of non-volatile flash memory space is used for firmware storage only, as it is rated at 10K duty cycles and would be quickly depleted if used for routine data storage. 4K of non-volatile electrically erasable/programmable read only memory (EEPROM) is used to store dynamic variables. 4K of volatile static random access memory (SRAM) is used for temporary storage of MESA data, until it can be stored in an off-chip Atmel AT45DB161D 16 Mb flash memory device rated at 100K cycles.

The ATmega128L has a full suite of external interface options. Eight channels of 10-bit ADC are used to collect voltage, current, and temperature telemetry. Two four-channel MAX4634 analogue multiplexors are used to accommodate a total of 14 EPS and TCS measurement points. The I2C interface is a two-wire serial interface used to control the VS6502 CMOS imager. The Universal Synchronous-Asynchronous Receiver/Transmitter (USART) ports serve as hard-wired umbilical (UMB) ports during software development, testing, and integration then interface with the radio and GPS module during flight. The SPI bus is used to control the MESA DAC and ADC devices, in addition to the external flash memory chip.

All 53 programmable interface pins are used for control and data acquisition of the MESA payload, CMOS imager, radio, GPS module, sun sensors, real-time DS1302Z clock with battery backup, and separation switch. One line is configured as a pulse-width modulated (PWM) clock for the imager.

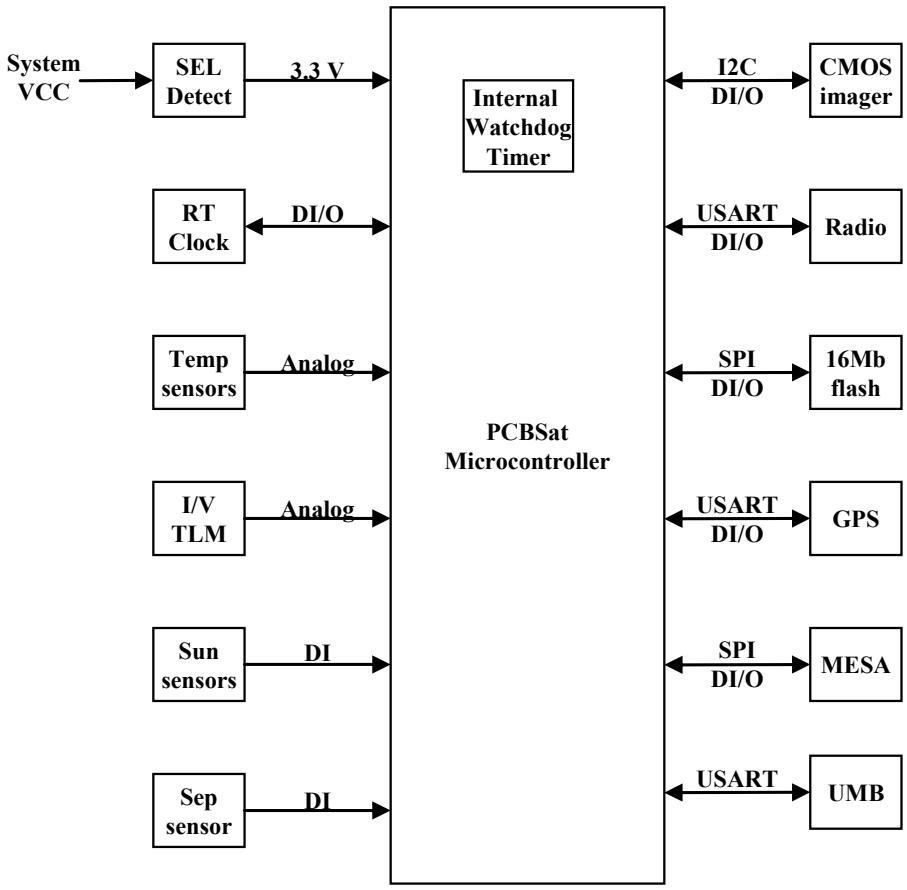

Figure 6-21. DH Subsystem Block Diagram

Similar to SpaceChip, the TID and SEE induced by the radiation environment is a concern. The TID hardness of all components is verified to 20 krad (SiO_2) as reported in Section 7.2.5. 1.6 mm aluminium plates are added behind the solar panels not only for passive thermal control discussed in Section 6.8, but also for a minimum amount of TID shielding. SEU cannot be prevented, but will be tolerated in terms of possible faulty data or incorrect firmware operation. If the SEU causes the microcontroller to go into an indeterminate state, the internal watchdog timer will reset the microcontroller. Similarly, the microcontroller monitors the devices in the MESA payload, CMOS imager, GPS module, and radio. If any of these devices fail to respond, the microcontroller power cycles them. In the event of an SEL, the external MAX892 current monitor will power cycle the microcontroller if excessive current is detected. Similarly, the microcontroller will monitor the expected power levels depending on the mode of operation and reset any attached device that causes excessive current draw induced by an SEL.

The firmware for the project is approximately 2000 lines of code written in the ANSI C language. The compiled binary file requires 15% of the flash memory and 4% of EEPROM. A real-time operating system is not required, as the code is written at a device driver level with hardware interrupts, which ensures real time operations for the primary task of payload collection with accurate time stamping.

The basic flowchart of the software is shown in Figure 6-22. When the RBF switch is removed, or any other event such as a SEU-induced watchdog reset or SEL-induced hardware reset, the firmware enters into a 10-second diagnostics hold where all subsystems are shut down. If a maintenance command is received via the GSE umbilical (UMB) interface, then the firmware remains in UMB mode to perform basic diagnostic tasks until power cycled.

If no input from the UMB is received, the firmware enters into a hardware sleep mode, waiting for the spacecraft separation indication. During this time, the ATmega128L uses very little power and continues to disable all subsystems, most importantly the radio. Once the separation indication is received, the firmware enters into an orbit diagnostics mode, where basic telemetry results are checked. The radio is powered on with the lowest transmit (TX) level of one milliwatt RF, as the constellation will only have sub-meter separation at this point. Once basic diagnostics are complete, a small TLM status heartbeat packet is transmitted on occasion through the ad-hoc mesh network to the supporting relay satellite. At this point, the ground station can acquire the relay satellite and determine the separation and health status of the constellation.

Once the commissioning phase of the mission is completed, the ground station can issue a normal operations command, where the firmware continuously loops through the right hand side of Figure 6-22. During eclipse, the GPS module asserts a hardware interrupt, where this loop is suspended, so that immediate payload measurements can be made, time stamped, and stored. The ground station can allow autonomous data collection or task on command hereafter.

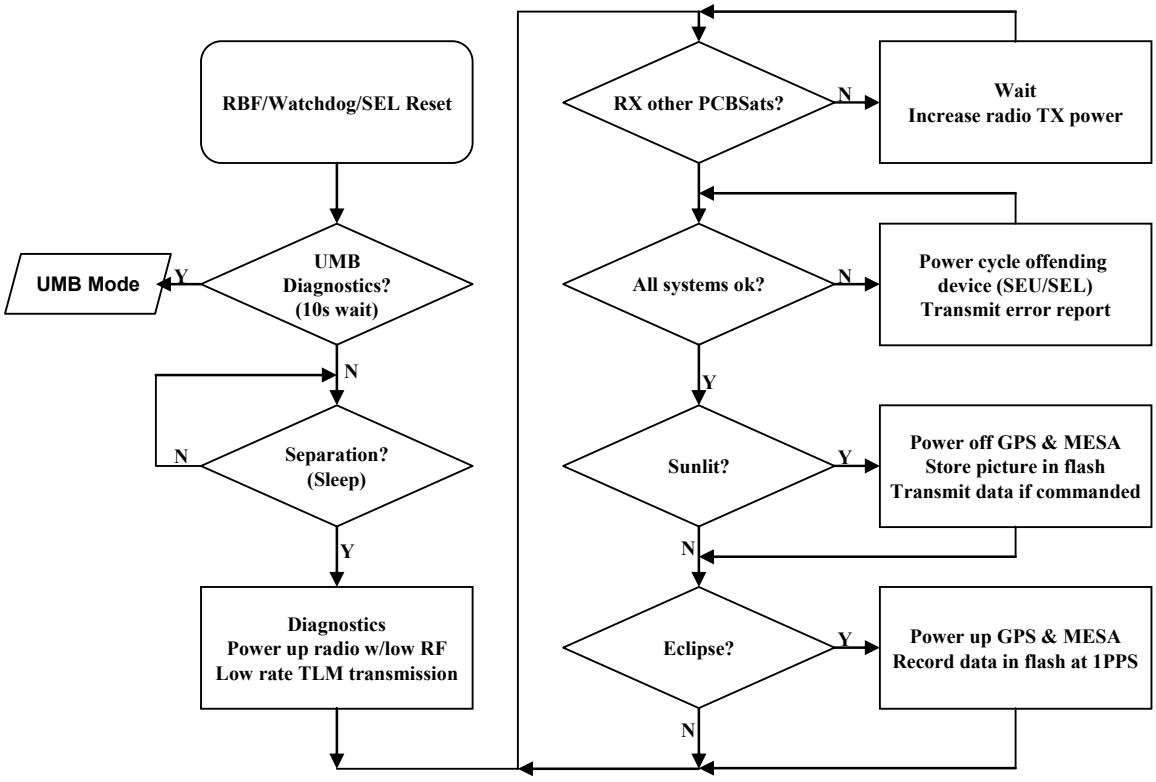

Figure 6-22. PCBSat Firmware Flowchart

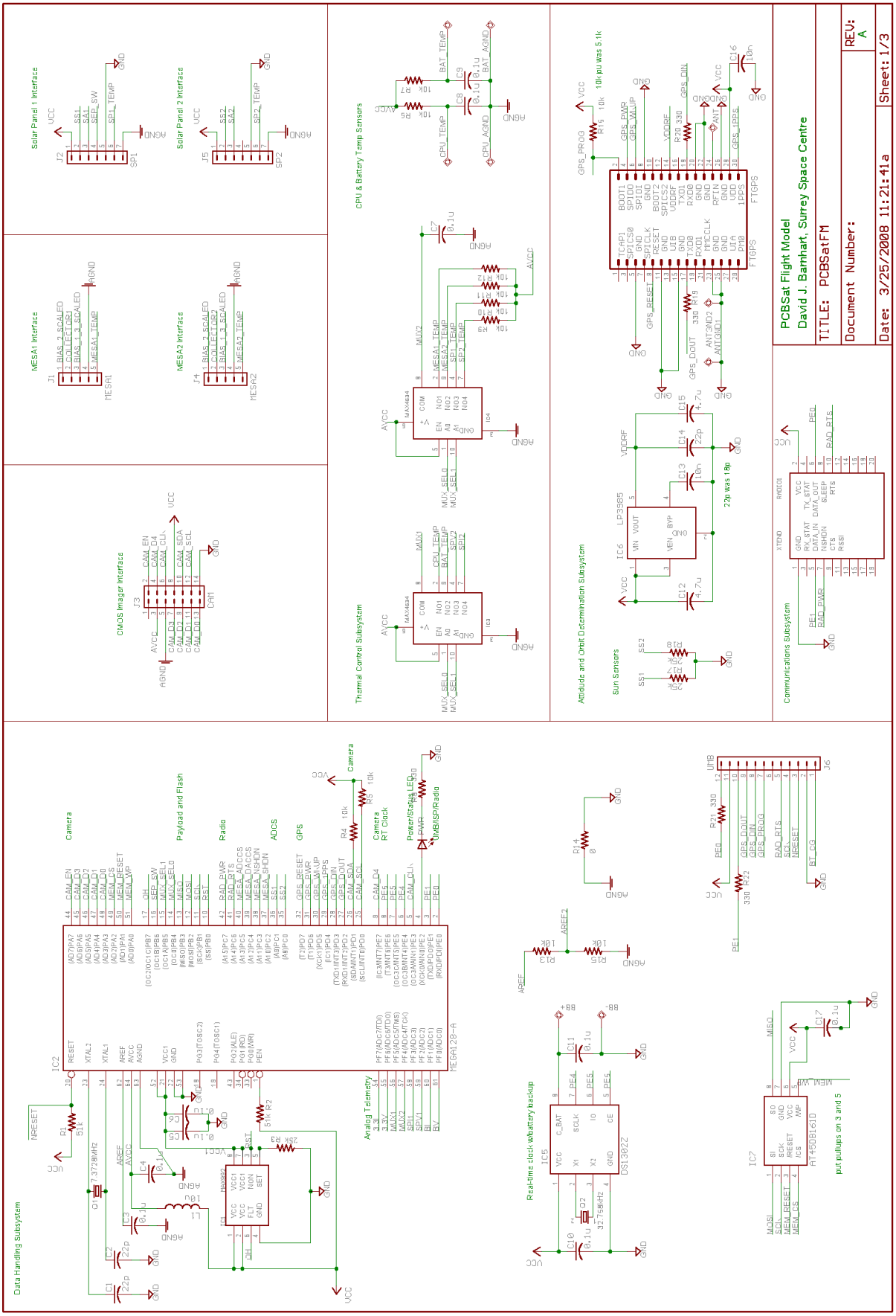

Figure 6-23. PCBSat DH Subsystem Schematic

6.6 Communications Subsystem

The PCBSat Communication subsystem is one of the key elements of the design, as the communication range is a significant parameter to trade off in the space sensor network. In addition, unlicensed frequency bands, low-power requirements, and built-in ad-hoc networking are of utmost importance. Table 6-7 summarizes the solutions investigated for PCBSat.

Table 6-7. Communication Subsystem Options

Specification	ATR 2406 [226]	XBee Pro [227]	XTend [228]	MHX-2400 [229]
Vendor	Atmel	MaxStream	MaxStream	Microhard
Mesh Network	No	Yes	Yes	No
ISM Band	2.4 GHz	2.4 GHz	900 MHz	2.4 GHz
Cost ($)	8	32	179	750
Size (cm)	3×6	2.4×3.3	3.7×6.05	5.3×8.9
Mass (g)	1	4	18	75
CPU use	50%	No	No	No
External parts	21	0	0	0
Voltage (V)	3.3	3.3-5	3.3-5	5
Data rate (kbps)	9.6-122.88	9.6-115.2	9.6-115.2	2.4-115.2
RF (mW)/dBm	2.5/4	60/18	1000/30	1000/30
Advertised Range (km)	0.3	1.3	32	100
RX current (mA)	57	55	80	210
TX current (mA)	42	214	600	550
TX efficiency	1.3%	6.7%	25.3%	36.4%

The single-chip ATR2406 transceiver is used on PCBSat RevA, but requires excessive CPU support, has low TX efficiency, low range, and requires numerous passives and significant PCB area [226]. The XBee, not shown in the table, has similar performance to the ATR2406 and has its own processor. The XBee Pro offers a small improvement in efficiency and range and supports mesh networking [227]. It is obvious that longer range extends the mission lifetime, due to the natural separation of PCBSats in orbit as discussed in Section 3.3.4.3. Even though the MHX-2400 is the CubeSat Kit baseline radio [229], the XTend is superior in terms of size, mass, cost, and offers low voltage (3.3 V) operation but with a reduced RF power output of 500 mW [228]. The XTend is shown in Figure 6-24 and Figure 6-25.

Quarter-wave antennas for 900 MHz are approximately 8.2 cm. Deployable antennas will achieve the highest gain. Two common techniques discussed in Section 3.3.4.3 are the use of deployable antennas using common steel tape measure blades released by monofilament fishing line. The deployed positions of the four antenna elements antennas are shown in Figure 6-27. These antennas double as passive attitude control, discussed in the next section.

The maximum range possible between satellites is calculated with Equations 4.8 then 4.7. Using the XTend specified values of transmitter power (P_t = 500 mW), frequency modulation (minimum

E_b/N_o = 13.3 dB, desired E_b/N_o = 23.3 dB), true RF datarate with protocol overheads included (R = 10000 bps), a free space loss L_s of -135 dB is found. This assumes transmitter and receiver antenna gains of -2.7 dBi as found through hardware testing in Section 7.2.3 ($G_t = G_r$ = -2.7 dBi), Boltzmann's constant ($k = 1.381\times10^{-23}$ J·K^{-1}), and typical system noise (T_{sys} = 28.3 dB·K). With a specified frequency (f = 915 MHz) and corresponding wavelength (λ = 32.8 cm), the theoretical maximum range S is found to be 147 km. The antennas are implemented as a monopole with passive mirror element and integrated ground plane, so the radiation pattern is near omnidirectional, except directly to the rear of PCBSat. Details of initial RF testing and further considerations are discussed in Section 7.2.3.

Figure 6-24. Digi XTend Radio Modules [228]

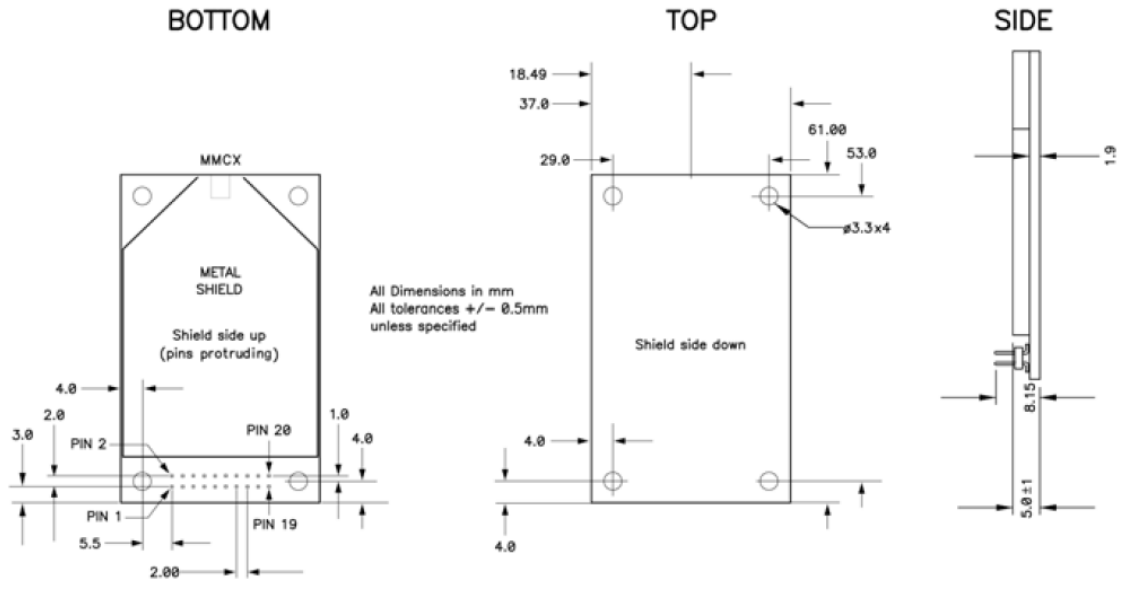

Figure 6-25. Digi XTend Radio Module Dimensions [228]

As wireless sensor networks have proliferated, so has the research into the various supporting network protocols [3]. For example, XMesh is an ad-hoc, multi-hop, mesh networking library for the TinyOS operating system for terrestrial wireless sensor nodes that are available commercially [230]. Similarly, MeshX is a mesh networking protocol that is embedded in the firmware of

MaxStream RF radios, such as the XTend [231]. MeshX is an ad-hoc, self-healing, peer-to-per architecture. Routing overhead will be reduced by using a reactive protocol similar to Ad-hoc On-demand Distance Vector (AODV). Rather than maintaining a network map, routes are discovered and created only when needed. Only the destination node replies to route requests and gives acknowledgements [231]. Once deployed, PCBSat will use MeshX for the crosslink network protocol. The relay satellite will poll each PCBSat in turn for its stored payload and telemetry data. Additionally, the PCBSat firmware will dynamically determine the appropriate RF transmission strength to save power based on the acknowledgement status as discussed in Section 6.5. An example MeshX network topology is shown in Figure 6-26 [228].

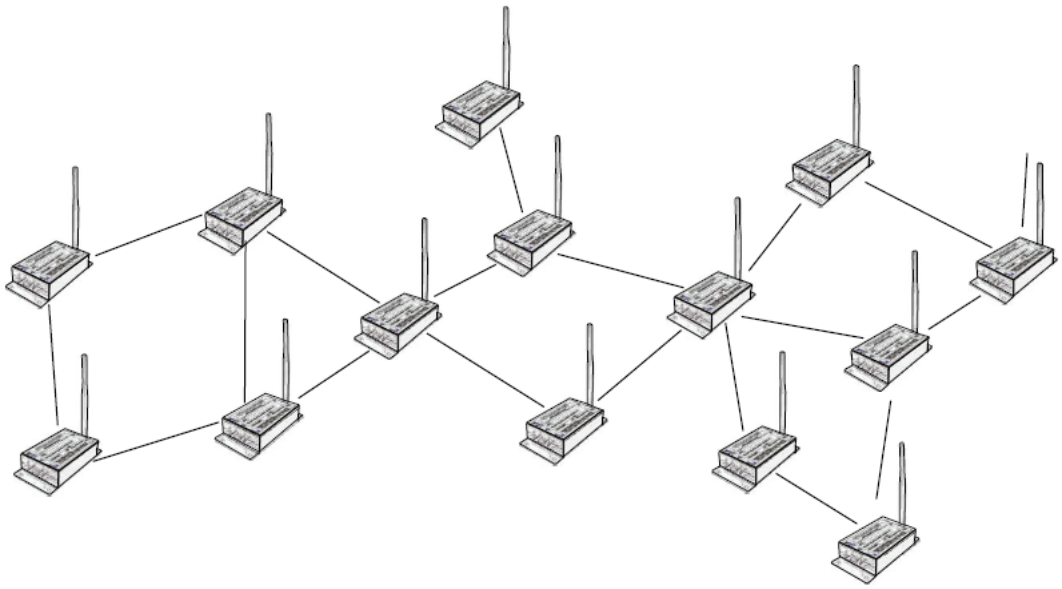

Figure 6-26. Digi MeshX Network Topology [228]

6.7 Attitude and Orbit Determination and Control Subsystem

Various ADCS options are available at this scale depending on the mission and sensor requirements. A miniaturized closed-loop control system is possible, based on magnetometer and/or gyroscopic attitude determination and magnetorquer or even reaction wheel control. However, no attitude control is required by the payload for this mission with the MESA sensor in an electron-sensing configuration only. If the MESA sensor is to detect ambient ions in LEO, only rough attitude control is required.

A passive attitude control system is proposed for the first PCBSat mission. The deployable antenna concept pictured in Figure 6-27 and discussed in Section 3.3.4.3 can provide rough attitude control by acting as a shuttlecock [181]. To improve the aerodynamic stability, the CG of PCBSat is purposely set toward the front corner, which is the one furthest from the antenna

mounting point, by the strategic placement of the MESA sensors, radio, and battery. The deployed antennas shift the centre of pressure (CP) toward the rear corner of PCBSat. To dampen oscillations, a permanent magnet could be used, but MESA cannot tolerate a strong magnetic field whilst taking measurements. In this case, a magnetorquer with PWM actuation satisfies this requirement. Crude attitude determination is accomplished with two cadmium sulphide (CdS) sensors, one on each side. MEMS accelerometer and gyro ICs could be added to evaluate the passive ADCS strategy on orbit.

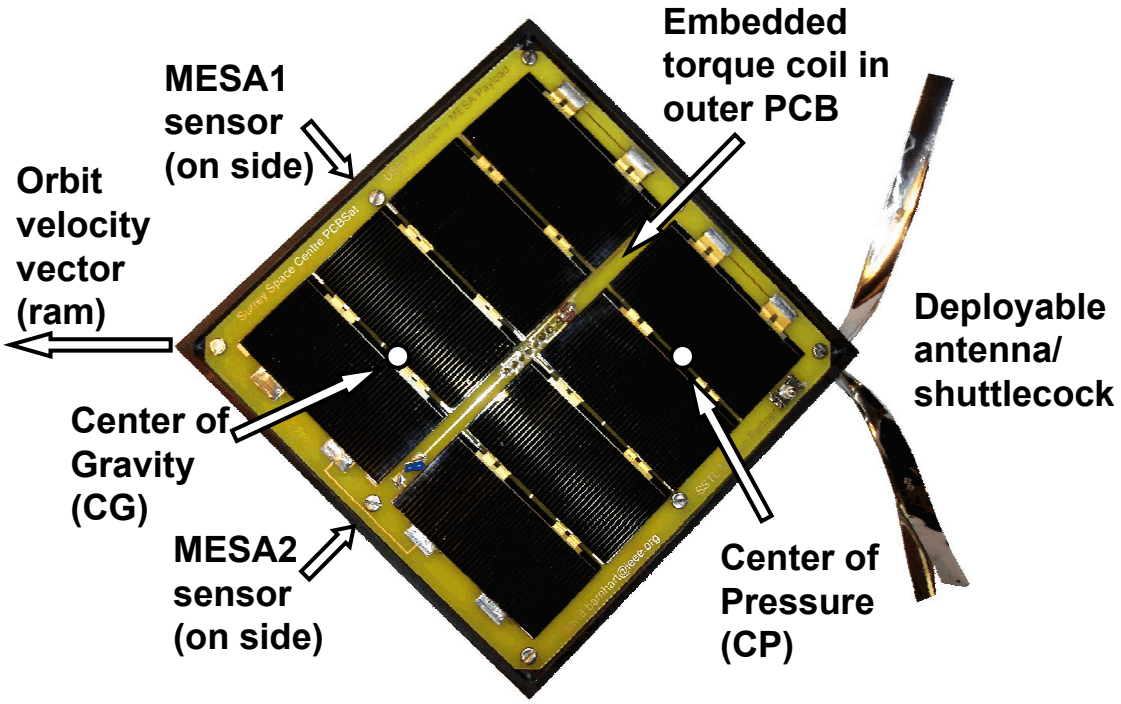

Figure 6-27. PCBSat Passive ADCS Features

The MESA data captured at one sample per second, must be position and time stamped. The only reasonable way to accomplish this is with an onboard GPS receiver. Postage stamp sized GPS receivers, such as the Fastrax iTrax-03S [232], and miniature antennas, such as the Sarantel GeoHelix-SMP passive antenna [233] (both shown in Figure 6-8), have only just emerged during the course of this research. This combination requires 100 mW of power. The one pulse per second output is connected to the ATmega128L's interrupt capture port providing precise internal time stamping of events. Ceramic surface-mount antennas are also possible, but require tedious trial-and-error in the design of the supporting PCB ground plane in addition to routing the RF signal from the outer PCB to the core. One complicating issue is that terrestrial GPS receivers cannot be used directly for space applications [74], which is fully explained in Section 7.2.4.

6.8 Thermal Control Subsystem

The orbital thermal environment is an issue that is often the least understood and most overlooked in small satellite design. The vacuum of space introduces unique thermal control challenges, as the convective heat transfer with the air in the terrestrial environment mitigates non-space system thermal problems. The spacecraft structure, in addition to ensuring the satellite survives launch, can be purposely designed to ensure a tolerable thermal environment. Specific thermal requirements can be met with active thermal controls. For very small satellites in particular, the challenge is twofold: the small area exposed to the sun reduces thermal absorption and internally, high-dissipative loads can be difficult to radiate, again due to the available surface area [234].

As PCBSat has a relatively low power consumption, the second case is not an issue. However, keeping the satellite sufficiently warm is dictated by the most thermally sensitive devices, typically the battery. The operating range of all components used is given in Figure B-2, p. 206. Six thermistors sense the temperature of the solar arrays, MESA sensors, battery, and CPU.

A first-order thermal analysis is accomplished, similar to the one for SpaceChip given in Section 4.9. The basic assumption is that PCBSat is a large, thin, solar panel. This gives an absorptivity α of 0.805 and emissivity ε of 0.825 of both sides. The Earth angular radius and view factors are the same as before, given an altitude of 500 km (ρ = 68 degrees, F_p = 0.86, and K_a = 0.99). For the hot case, the solar flux G_s is 1418 W·m^{-2}, albedo *alb* is 35%, and Earth infrared q_I is 258 W·m^{-2}. Assuming a Stefan-Boltzmann constant σ of 5.67×10^{-8} W·m^{-2}·K^{-4}, a hot case thermal equilibrium temperature of +77 °C is reached, using Equation 4.11. Similarly, using a cold Earth infrared q_I of 216 W·m^{-2} and Equation 4.12, a cold equilibrium temperature of -63 °C is reached. These extremes only bound the problem.

Ideally, the interior of the spacecraft should be kept near room temperature, around 25 °C, to reduce thermal stress on the electronic components. One simple method of achieving this would be to fill the interior cavity with space-qualified paraffin [184], which would absorb heat in the sun then keep the interior warm during the eclipse. However, there are practical design complications with liquid material containment. A simpler approach is taken, where an aluminium plate is placed behind the outer solar cell PCBs that is insulated physically from the core PCB with Delrin spacers as illustrated previously in Figure 6-5. These plates absorb the heat through conduction, and then radiatively warm the core PCB, battery, radio, and GPS, during the eclipse and prevent overheating in the sun, as their emissivity coefficient is only 0.03-0.04. A network analysis of the thermal environment is presented in Section 7.2.6.

6.9 Ground Support Equipment

Miniaturized GSE is required to support development, testing, and pre-flight operations. A custom GSE PCB shown in Figure 6-28 is used to charge the battery, check PCBSat status, and upgrade the firmware in FLASH memory of the CPU, GPS module, or radio module. It provides the interface between PCBSat and standard devices without requiring these large connectors to be placed on the core PCB. Figure 6-28 shows the connection of an AVR ISP programmer, a USB to TTL interface, and a power supply/battery charging adapter. The location of the maintenance port on PCBSat is placed such that it can be reached via the P-POD access panels.

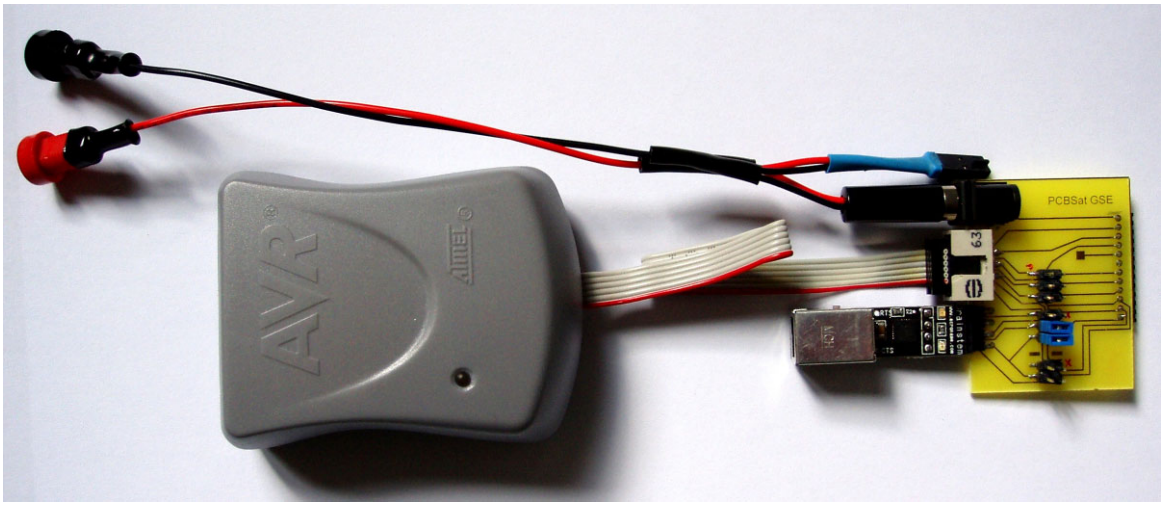

Figure 6-28. PCBSat GSE PCB

6.10 PCBSat Flight Model Fabrication

The PCB CAD tool selected for this project is EAGLE 4.11 (Easily Applicable Graphical Layout Editor) [235]. When a version of the PCB is complete, the Gerber and drill files are generated and first checked with Pentalogix Viewmate. The PCBs are then fabricated any PCB house.

Nearly all components are procured from a single vendor. The only exceptions are for the GPS module, GPS antenna, and a few ICs, which must be purchased directly from specialty vendors when in small quantities. When possible, all parts are ordered and acceptance tested by a fit check using a paper version of the PCB. This eliminates common sizing errors that occur during the creation of a new PCB library component. Once the prototype PCB is received, it is soldered by hand and incrementally tested. When a final configuration is reached, it can be sent off for mass production.

The structure is originally designed by hand, then an as-built drawing of the structure is accomplished as shown in Figure B-9, the last page of this thesis. The University of Surrey machine shop crafted the structures on a non-computer numerical control (CNC) mill. However,

these simple structures, now specified in an industry standard file format, can be quickly machined and mass-produced on CNC mills, or even injection moulded given a high enough quantity.

Finally, hand-touch labour is required for two items: the solar cells and the deployable antenna. Once the tuned antenna length is found, it can be mass-produced as well. Solar cells naturally require finesse, as they are fragile. In addition, contacts must be ultrasonically welded and coverglass applied. Finally, they must also be screened for functionality then classified by current rating to be sure each panel has maximum power output. This process is described fully in Section 7.2.2, which doubles the cost of the cells due to the labour involved.

The major components of the flight model prototype are shown in Figure 6-29. The Delrin insulating spacers can be seen, one for each side of the core PCB. The aluminium plates and solar arrays are also shown. Mock-ups of the MESA sensors are shown for scale, as the PCBSat-specific configuration is still in fabrication. The mounting hardware is not shown.

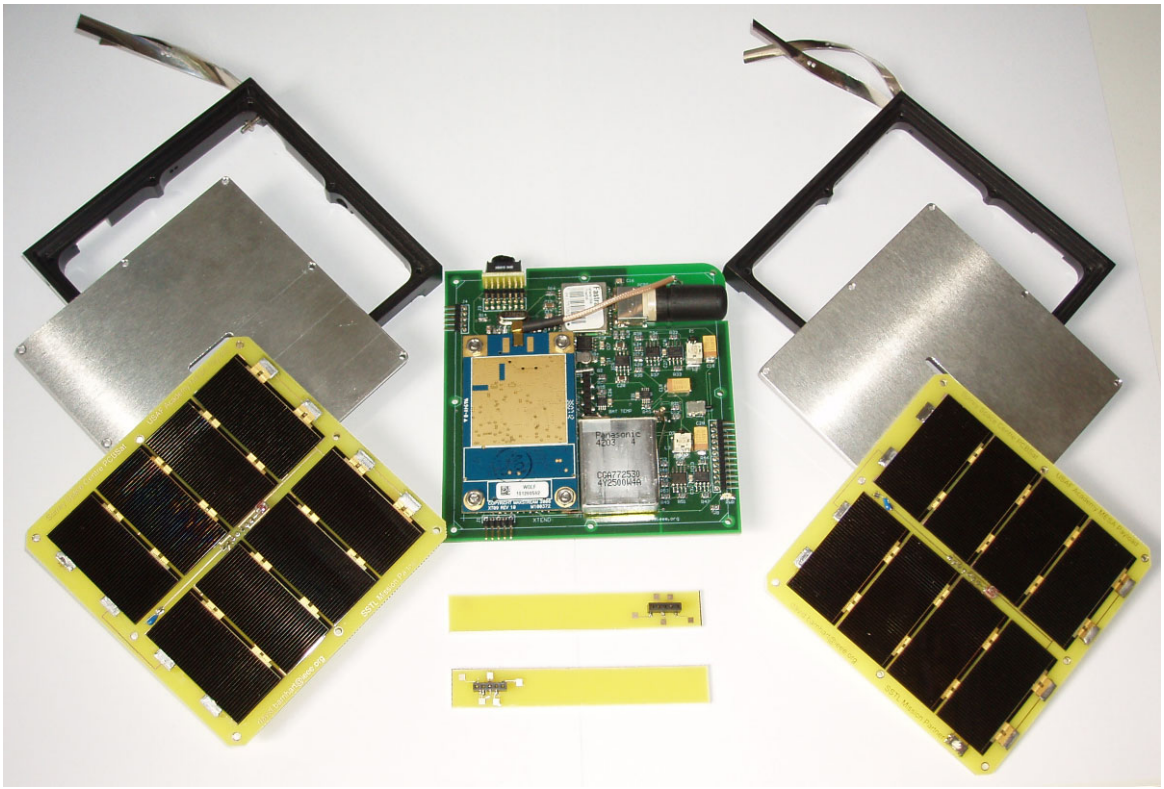

Figure 6-29. PCBSat Flight Model Components

Figure 6-30 shows the assembled flight model with the RBF plug inserted. The design of the Delrin spacer allows for the stacking of PCBSat in a P-POD without damaging the components on each solar array face. The separation switch is on one of the solar array faces and is spaced exactly for proper contact when stacked. The GSE PCB can be inserted whilst in the P-POD for final verifications.

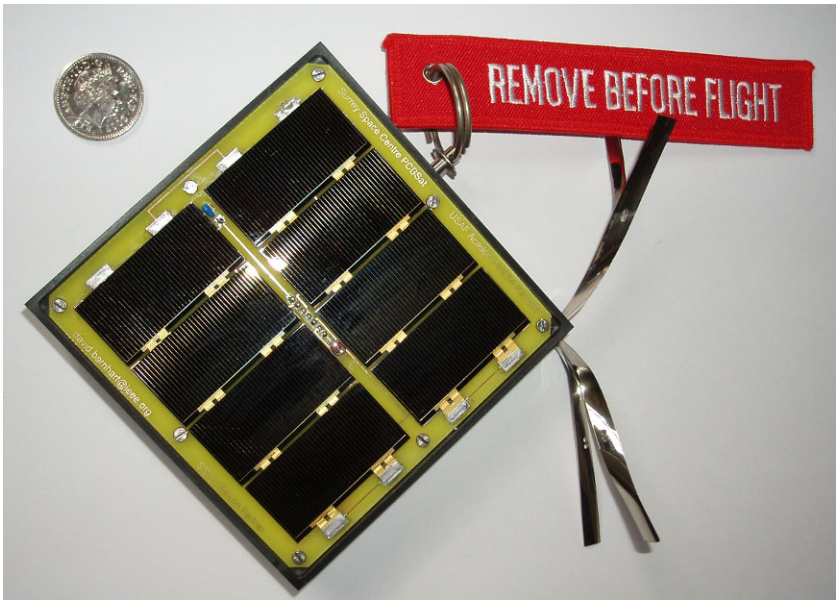

Figure 6-30. PCBSat Flight Model Assembled

6.11 Summary

The PCBSat satellite miniaturisation approach is presented, focusing on determining the smallest practical satellite within the context of space sensor networks. PCBSat is based on a satellite-on-a-PCB approach, which represents the strategy of constraining the satellite systems engineering process to using COTS components, fabrication processes, and deployment systems.

A flight model prototype is designed and built, targeting application in the Chapter 3 case study mission to demonstrate the merit of this approach. Four revisions have produced a final configuration of 10×10×2.5 cm and 311 grams. A total of eight FR4 PCBs, two 6082-T6 aluminium plates, and two Delrin spacers are the primary structural materials, which serve to provide the P-POD compatible launch vehicle interface and protect the interior components from total radiation dose and thermal extremes. The MESA payload sensor plates are mounted on two adjacent sides, whose mutual corner generally points in the velocity vector due to placing the CG in front of the CP, enhanced by deployable antennas conveniently placed. The EPS provides sufficient power to charge the batteries and enable the radio during the sunlit portion of the orbit, so that MESA and GPS can operate during the eclipse. The DH subsystem collects payload and telemetry data at all phases of the mission, which is forwarded on command through the ad-hoc mesh network to the co-orbiting relay satellite.

The novelty of this approach lies in the near-subsystemless implementation with low-cost technology. As satellite miniaturisation progresses, the subsystem interface requirements naturally vanish whilst the multifunctional aspects start to dominate. Although targeted to a case study mission, PCBSat is applicable to a wide range of missions as discussed in Chapter 2.

Chapter 7

7 PCBSat Characterisation and Test Results

This chapter presents the results of functional and environmental testing of the PCBSat flight model prototype, which is targeted for the case study mission in Chapter 3. PCBSat is subjected to a number of evaluations, spanning from full functional testing and characterisation in Section 7.1 to environmental testing in Section 7.2. Section 7.3 compares the results to mission requirements.

7.1 Functional Characterisation and Testing

Functional characterisation is essential to determine the baseline performance of any system. Once the actual performance is determined, a set of routine full functional tests and expected results are developed. The full functional test is then used before, during (in some cases), and after all environmental tests.

The process of initial assembly and characterisation has been updated during each prototype design. It is essential that the set of required evaluations be determined in concert with the system design. Table 7-1 presents the general flow of the system build-up indicating incremental evaluations and results. The component values shown can be observed in the PCBSat core PCB schematics, shown previously in Figure 6-12, Figure 6-19, and Figure 6-23. The positions of the components are shown in Figure B-5 and Figure B-6 on p. 208. These results are back annotated in the Chapter 6 design process.

Starting with the GSE PCB, it is built up and tested for continuity whilst plugged into the bare core PCB. This ensures that no faults exist which could cause damage whilst populating and testing. As each functional group of components is added, the ATmega128L is programmed via ISP, adding the required support code in firmware. Various parameters are checked as applicable, but almost always, the baseline current draw (Idraw) is measured. If the added components can be enabled by command, the additional current draw is measured (+Idraw), then disabled before proceeding. Calibration of TCS and EPS telemetry points occurs at steps 10 and 13, respectively.

The full functional test is a product of the initial characterisation results. Several internal diagnostics take place automatically in firmware; however, some basic checks are performed as indicated in Table 7-2. All of these tests are performed throughout environmental testing and launch vehicle integration, but only a subset is possible once stacked in the P-POD.

Table 7-1. PCBSat Initial Assembly and Characterisation

Build	Components	Test	Result
1. GSE PCB	J1-7	Continuity	PASS
2. Core PCB	-	PWR/GND short	PASS
3. Core PCB	J6	Core/GSE Continuity	PASS
4. Microcontroller	C1-6, R1,2,4,5,13-15,21,22, IC2, L1, Q1	ISP	PASS
		Clock freq.	7.6 MHz
		UMB	PASS
		Idraw	9.1 mA
5. RT Clock	C10,11, Q2, IC5, BB+/-	UMB	PASS
		Clock freq.	32.7 kHz
		+Idraw	9.1/0 mA
6. Status LED	R8, LED	ISP	PASS
7. SEL monitor	R3, IC1	ISP	PASS
8. External flash mem.	C17, IC7	ISP	PASS
9. Comm	XTend header	RF	PASS
		+Idraw	9.1/80 mA
10. TCS	C7-9, R6,7,9-12, cpu_temp, bat_temp, IC3,4	ISP/Cal.	PASS
		+Idraw	9.1/0 mA
11. GPS	C12-16, R16-20, IC6, GPS	ISP	PASS
		+Idraw	9.2/37 mA
12. Camera	J3 assembly	ISP	PASS
		+Idraw	9.2/30 mA
13. EPS TLM	C22-26,29-31, R23-31,40,42,43, 45, IC10,11,14,15	ISP/Cal.	PASS
		+Idraw	9.9 mA
14. EPS Voltage Regulator and Battery	C20,21, R44, IC9, RBF switch	Vcc	3.3 V
		+Idraw	10.0 mA
		Eff.	92%
15. EPS PPT/BCR1	C18,19,27, R32-39, IC8,12, D1, L2	+Idraw	10.1 mA
		Eff.	82.7%
16. EPS PPT/BCR2	C28,32, R46-53, IC13,16, L3, D2	+Idraw	10.2 mA
		Eff.	82.7%
17. MESA +12V	C39-42, IC20, L5, D4	+Idraw	10.2/20 mA
18. MESA -12V	C47,48,52,53, IC25, D9, L6	+Idraw	10.2/19.2 mA
19. MESA collector inst.	R54-60,63,64, IC17,18	+Idraw	10.6/8.7 mA
20. MESA collector ops.	C43-46, 49-41, IC21-23, D5-8	+Idraw	12.8/27.6 mA
21. MESA bias ops	C54-60, R70-93, IC26	+Idraw	14.6/0.3 mA
22. MESA all on	-	+Idraw	14.6/71.4 mA
23. Top PCB	J6, R6, sep_sw, SP1_temp, P1-8	+Idraw	14.8/0 mA
24. Bottom PCB	J4, R1, SP2_temp, P9-16	+Idraw	15.0/0mA

Table 7-2. PCBSat Full Functional Test

Test	Action	Expected Results
1. Power up	RBF removed, sep toggled	Idraw=15 mA
2. DH	Self-diagnostics, clock set	PASS
3. Comm	Enable radio, verify RF mesh	PASS, Idraw=95 mA
4. EPS testing	Illuminate panels, check TLM	PASS
5. GPS	Enable GPS, go outside	Lock in 30 sec, Idraw=52 mA
6. TCS testing	Touch each temp sensor	Variation in TLM
7. MESA testing	Enable MESA, ramp plate V	Appropriate variation in TLM
8. Camera testing	Enable camera, capture image	Transmit data file

7.1.1 P-POD Compatibility Testing

A simple fit check of a PCBSat flight model mock-up is accomplished. Both the Test Pod, shown in Figure 7-1, and the P-POD MkII, shown in Figure 7-2, are used to determine PCBSat's compatibility. The PCBSat concept has been verbally accepted by the governing CubeSat organisation provided a dedicated P-POD is procured [236].

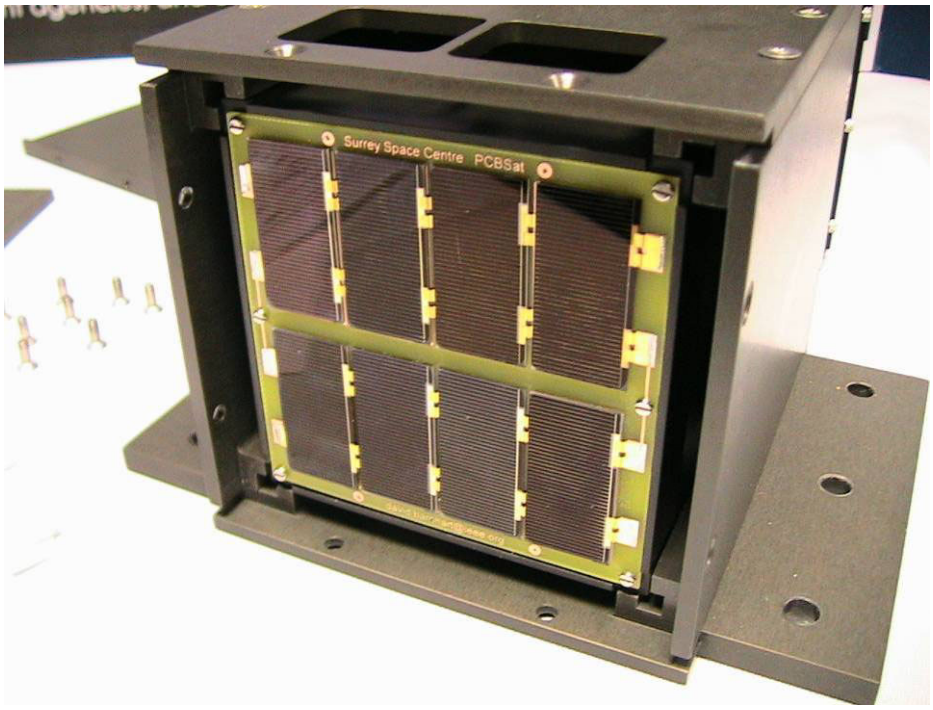

Figure 7-1. Fit Check of PCBSat in Test Pod

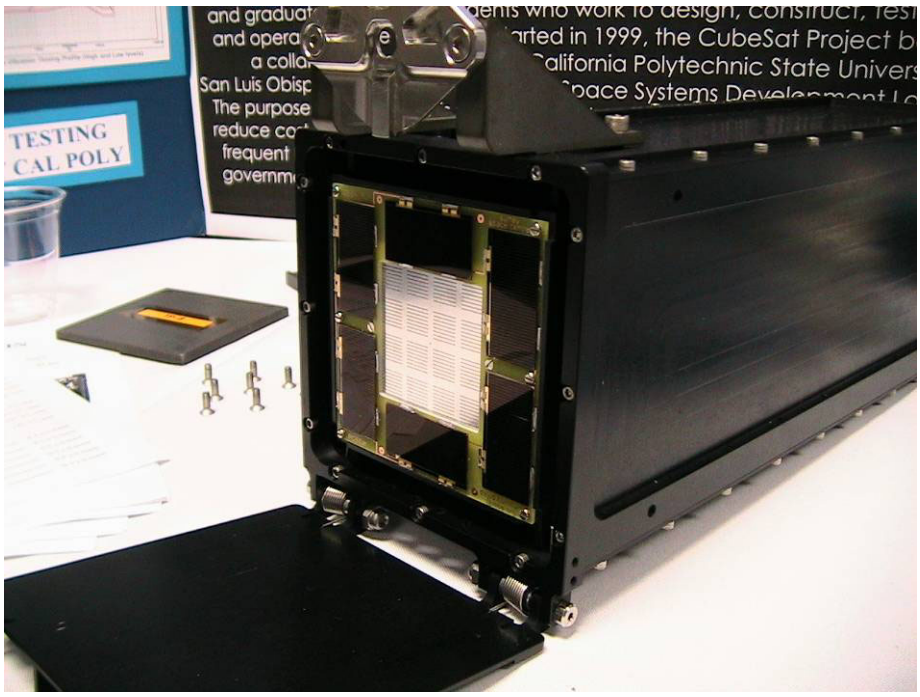

Figure 7-2. Fit Check of PCBSat in P-POD MkII

Before any satellite can participate in a P-POD launch, it must meet all the interface requirements. Some of the requirements can be relaxed when the customer is using the entire P-POD, as there is no risk to harming any co-deployed satellites from other customers. There is always the requirement to impose no risk on the launch vehicle operations and primary payloads. A summary of P-POD and CubeSat requirements and status is given in Table 7-3 [130]-[131].

Table 7-3. P-POD and CubeSat Launch Vehicle Interface Requirements [130][131]

Requirement	Comment	Result
1. 10×10×34 cm maximum size	1 CubeSat relay and 8 PCBSats	PASS
2. 1 kg/10 cm height	311 grams/2.5 cm exceeds this requirement by 20%, but overall by 13% with relay. There is margin in the P-POD design, so 3.4 kg is OK	Exception
3. A 6.5 mm protrusion allowed between rails	Allowance used for MESA	PASS
4. Centre of gravity at centre of mass	Staggered stacking required due to intentional CG offset for ADCS	PASS
5. All parts remain attached always	Only exception is dissolving monofilament line	PASS
6. Designed to minimise jamming	Bailing method with inter-fitting should prevent jamming	Not Tested
7. No pyrotechnics allowed	Fishing line deployment actuators	PASS
8. NASA approved materials used	Where possible	PASS
9. Rails must be smooth w/round edges		PASS
10. 75% of the rails must contact		PASS
11. Rails must be hard anodized	Cold welding not possible with Delrin/anodized aluminium combo.	Exception
12. Custom intersatellite separation springs may be used	Fishing line bailing method acceptable with dedicated P-POD	PASS
13. Structure material must have a thermal expansion similar to 6061-T6	Delrin thermal expansion coefficient is 120×10^{-6} vs. 1×10^{-6} for aluminium. Fit tolerance must be carefully adjusted.	Not Tested
14. Deployables must be self-restrained		PASS
15. Battery must be deactivated during launch by separation switch		PASS
16. Must use RBF switch or start with dead batteries	RBF used	PASS
17. Antennas can deploy NET 15 minutes after separation	Estimated one to two days	PASS
18. Transmitter may activate 15 minutes after separation at low power	Software controlled	PASS
19. Transmitter may activate 30 minutes after separation at full power	Will be longer whilst constellation is bailed	PASS
20. Frequency license or coordination must be approved prior to launch	Amateur and ISM frequencies used with prior coordination	PASS
21. Orbital debris mitigation plan must be filed	2.5 year lifetime exceeding 25 year deorbit requirement	PASS
22. Must pass standard random vibe test		Not tested
23. Must go through thermal bakeout		Not tested

7.2 Environmental Analysis and Testing

Solar, RF, AOCS, and radiation test results are reported in this section. Enquiries have been made for the use of vibration and thermal-vacuum facilities; however, this portion of the work has not been funded. Considerations for these tests are discussed instead.

7.2.1 Vibration Testing

The purpose of vibration testing in the case of PCBSat is to ensure quality workmanship. It is highly unlikely that this design approach has a low enough natural frequency to encounter resonance, as it resembles a typical PCB-based electronics tray used in many satellite designs [217]. The main consideration is that all fasteners are secured using epoxy or locking threads [218]-[219]. For PCBSat to fly on a P-POD mission, the following vibration test profile must be administered as shown in Figure 7-3, which is equivalent to the NASA General Environmental Verification Specification (GEVS) [130]. Optional vibration testing could be performed, such as shock testing up to 10 kHz and test to failure.

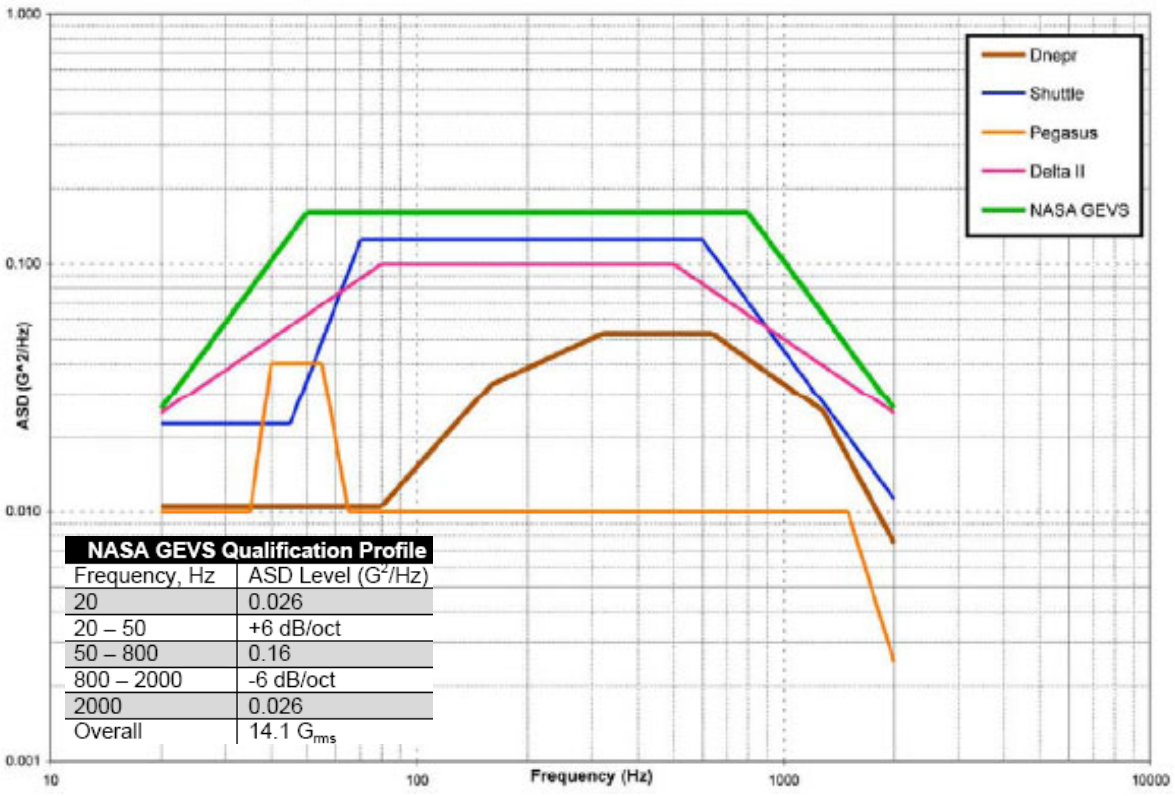

Figure 7-3. CubeSat Vibration Qualification Profile [130]

7.2.2 Solar Testing

The solar cells investigated in this research are single-junction 2×4 cm GaAs/Ge cells as discussed in Section 6.4. Although fully-assembled space-ready triple-junction cells are currently available for half the cost, the single-junction cells are made available at no cost from SSTL, as they are reject cells with minor imperfections. The cells are rated 18% efficient at 860 mV, 25°C, AM0 [222]. Two parallel strings of four cells in series are used as illustrated in Figure 6-18, delivering or 457 mA at 3.44 V (1574 mW). Each string should contribute about half of 457 mA (228.5). All solar cells used in the flight model are screened for quality workmanship, basic functionality, and peak power point current at AM0 illumination using SSTL's facilities as shown in Figure 7-4. Over 30 cells are screened and 16 selected as shown in Table 7-4. Cells are grouped by current rating for each string, as the lowest value in the string determines the maximum current flow.

Table 7-4. Solar Cell Screening

Cell	Short Circuit Current (mA)	Peak Power Current (mA)	Open Circuit Voltage (V)	Solar Panel	String	Panel Max/ Efficiency
EY069 103	252	**244**	1.025	1	1	
EY034 041	249	**242**	1.019	1	1	
EY043 025	248	**242**	1.023	1	1	
EY042 031	248	**241**	1.027	1	1	
EY064 063	252	**241**	1.021	2	1	
EY018 124	250	**241**	1.023	2	1	
EY024 048	250	**240**	1.018	2	1	
EY034 006	247	**239**	1.020	2	1	
EY031 008	250	**239**	1.019	1	2	
EY048 100	249	**239**	1.029	1	2	
EY024 066	247	**239**	1.022	1	2	
EY082 097	246	**238**	1.020	1	2	479 mA/18.8%
EY008 069	248	**238**	1.022	2	2	
EY024 067	247	**238**	1.019	2	2	
EY015 057	247	**238**	1.023	2	2	
EY008 077	243	**237**	1.024	2	2	476 mA/18.7%

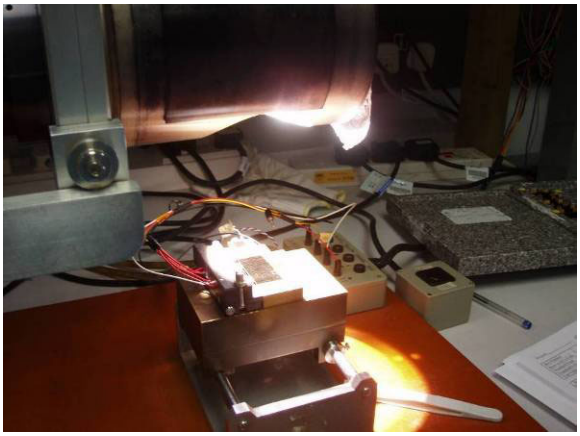

Figure 7-4. Solar Cell Screening Using AM0 Illumination

7.2.3 RF Testing

A range of initial RF characterisation is performed. Firstly, the proposed antenna design is tested and tuned by trimming at a proper antenna range. The results of this test are shown in Figure 7-5, noting the notch near the 915 MHz centre frequency goal. The best performance is achieved when the antenna is configured as a monopole with a parasitic mirror element. This is accomplished by connecting the active feed from the radio to one set of deployable antennas and the RF ground to the pair of aluminium shields leaving the other set of deployable antennas unconnected.

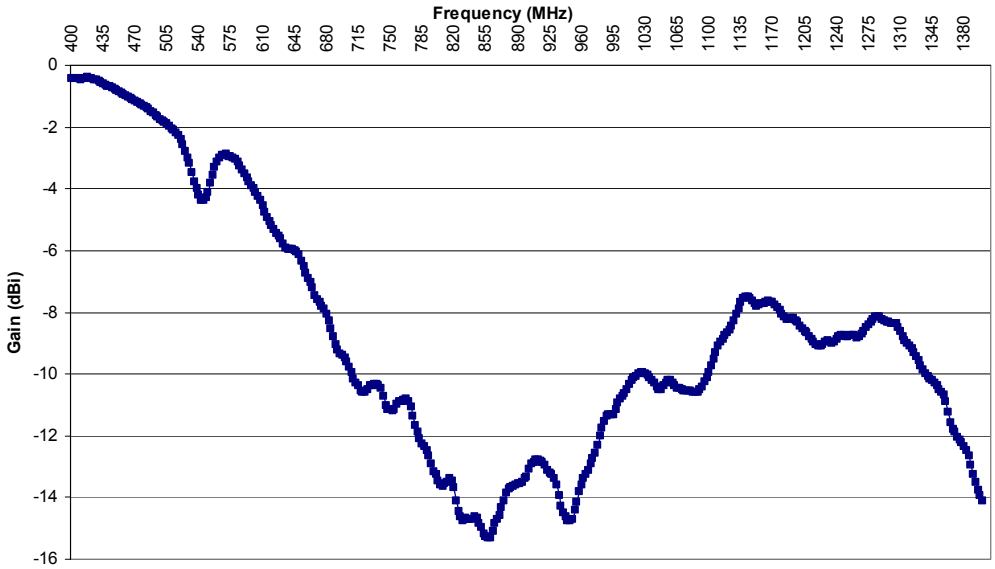

Figure 7-5. PCBSat Antenna Tuning

Secondly, the antenna pattern is determined at the RF range, using an automated turntable. The results of the circular and cross polarisation evaluations are nearly identical, so only one plot is shown in Figure 7-6 for both cases. The average antenna gain is -2.7 dBi.

The range of the XTend radios needs to be determined using this particular antenna configuration. This is a difficult proposition terrestrially, as the 902-928 MHz band is particularly noisy, especially in Europe. Global System for Mobile Communication (GSM) services in Europe and many other parts of the world use the 900 MHz band. In U.S., 900 MHz is the license-free ISM band. The XTend radio will soon be available in the 868 MHz ISM band for worldwide use, which will enable a better evaluation of the range terrestrially. Cabled testing with attenuators can be performed in an anechoic chamber, but at 500 mW output power, there is too much leakage to make this a valid test.

Finally, initial testing is performed on the MeshX protocol for the Digi XTend modules. The protocol is able to perform as designed, autonomously reconfiguring the routing paths as nodes drop in and out. More testing is required to determine the actual overhead of the protocol.

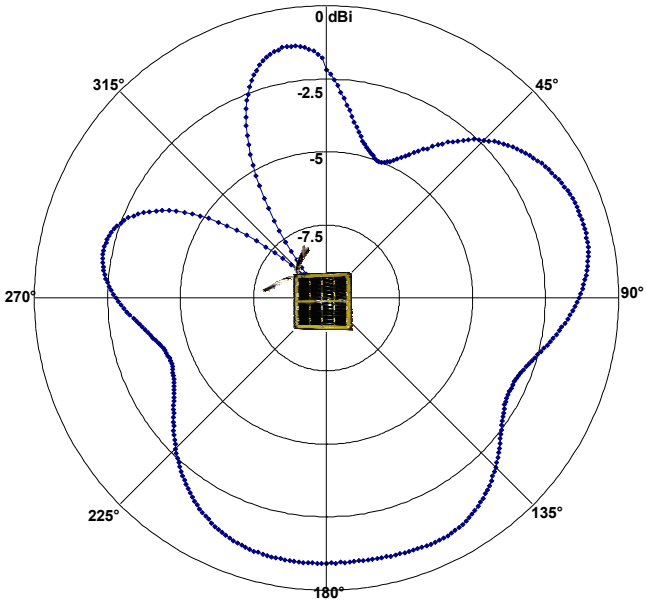

Figure 7-6. PCBSat Antenna Radiation Pattern

An initial investigation has been performed to determine the noise level of the 900 MHz band in space. The Amateur Satellite (AMSAT) AO-51 is tasked in 15 April 2008 to evaluate the received signal strength (RSSI) at the centre of the 900 MHz ISM band, which is 913.7 MHz, as shown in Figure 7-7 [237]. AO-51 is currently in a sun-synchronous LEO, with 98.1 degree inclination and 756 km altitude. Note that frequency modulation (FM) is used on the 2 meter antenna tuned for 1268.7 MHz. These results are interesting, but cannot be calibrated until a ground station can be tasked to transmit at this frequency with a high-gain antenna.

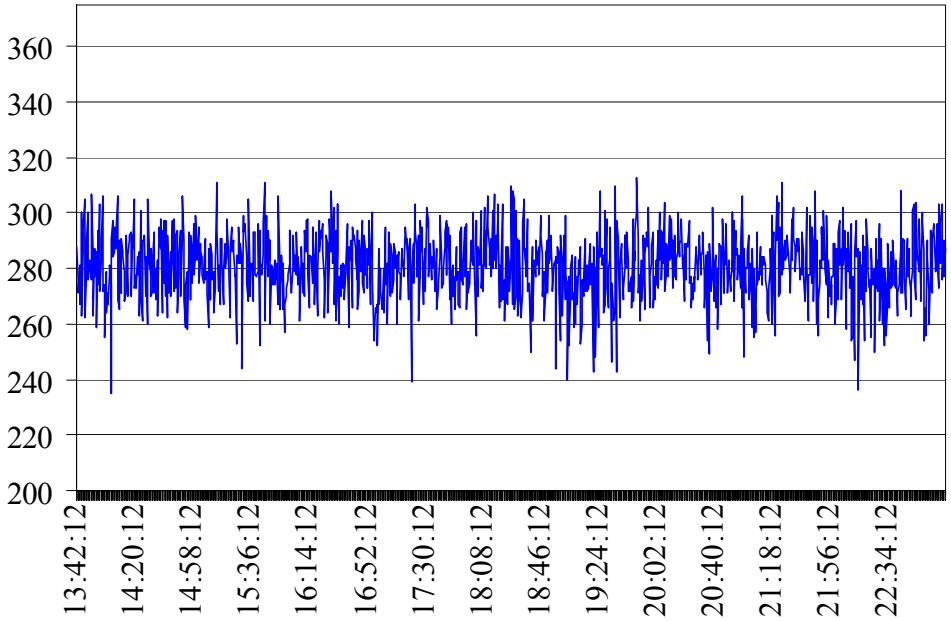

Figure 7-7. AO-51 RSSI at 913.7 MHz FM [237]

7.2.4 AOCS Testing

Terrestrial GPS receivers cannot be used directly in a space environment due to government limitations aimed at preventing hostile use. Limitations in firmware are required to prevent a valid fix when either the altitude exceeds 60,000 ft. or the velocity exceeds 500 m/s. Additionally, there are atmospheric corrections to improve terrestrial accuracy that must be removed. To verify these limitations, the iTrax-03S is tested in the GPS orbital simulator at SSTL. It is able to successfully track the satellites in view, demonstrating that the hardware can handle the Doppler shift experienced in LEO. As expected, it does not give a valid fix past the limiting points.

There are two possible ways forward. This simple test demonstrates that even postage-stamp sized GPS receivers have the hardware capability to operate in space. To make this happen, a special program would have to be pursued directly with the chipset manufacturer to modify the firmware for space use, in addition to acquiring the proper governmental approvals. Or, existing credit-card size receivers can be procured, which are typically export controlled by the host nation [74]. Open source solutions are also appearing from nations without such export controls [238].

Regarding the proposed passive shuttlecock ADCS technique, some initial thought has been given to testing terrestrially. Intuitively, a wind tunnel environment would verify the approach; however, these are not the same dynamics encountered on orbit. A reasonable simulation could be attempted in a vacuum chamber with a strategically placed subliming material that would blow past a suspended PCBSat with deployed antennae. A strain gauge could be used to determine the toque force on the spacecraft to determine if this approach is valid [239].

7.2.5 PCBSat Radiation Testing

Radiation and charged particles, whose fluence greatly varies with altitude, is a primary concern when flying COTS components in space [143]. Long-term exposure to radiation causes a degradation of performance and increased power draw due to the TID effect. This will not be a concern for short-lived missions like those that PCBSat will support in LEO, where the environment is only 1-1.5 rad (SiO_2) per day behind the typical shielding provided by the aluminium structure. Four mils of coverglass for the solar cells and a 1.6 mm aluminium plate are used on PCBSat to mitigate TID for the expected four-month mission.

SEE must be tolerated and handled using several strategies, as no amount of shielding will stop the high-energy particles that cause SEE. SEU rates of the order of 10^{-6} SEU bit^{-1} day^{-1} can be expected in LEO. For PCBSat, these errors will be accepted and erroneous data will be discarded. In the event that an SEU occurs in control logic, a watchdog timer will reset the system. A high current monitor will reset the hardware when an SEL is detected. These mitigation strategies are fully discussed in Section 6.5.

TID testing is performed on two prototype PCBSat units at the National Physics Laboratory in the United Kingdom. The purpose of this test is to determine if the selected COTS components are suitable for a mission in LEO. A total dose hardness of 5-10 krad (SiO_2) is typically desired for mission less than a year [143]. Determining SEE hardness is also important, but determining hardness levels through testing is very expensive, but can be partially mitigated using the techniques just discussed. Expected SEE hardness for various components is discussed in [143] and [240]. The test is performed over a period of 6 hours at a dose rate of 5.02 krad/hr (SiO_2). The ionizing radiation is 1.25 MeV gamma rays from a Co-60 source. The beam is kept at a fixed distance and nearly normal to the PCBs throughout the duration of the test. A picture of the irradiator and test fixtures is shown in Figure 7-8.

Figure 7-8. Co-60 Irradiator and Test Fixture

The first PCBSat is simply the PCB with the ATmega128L, crystal oscillator, and supporting capacitors mounted. The second PCB is populated as a complete Revision B PCBSat. 125 mils of aluminium spot shielding is applied over all integrated circuits on the second PCB. The shielding is not expected to reduce the dose, as this thickness and material is virtually transparent to the highly energetic gamma rays. However, this type of shielding is effective on orbit, where there is a wide spectrum of energies. The point of doing so is to ensure no dose-enhancement issues exist.

Both units are remotely powered with 3.3 V DC (measured at the components) and the current is monitored throughout. The power supply is used as the normal 3.3 V system regulated voltage (VCC/ICC) input for the first prototype. On the second PCB, it is used to simulate solar power input (SPV/SPI) to the PPT/BCR circuit, although no battery (BV) is used. In addition, the second prototype transmitted telemetry via the wireless link throughout the test, as shown in Figure 7-9.

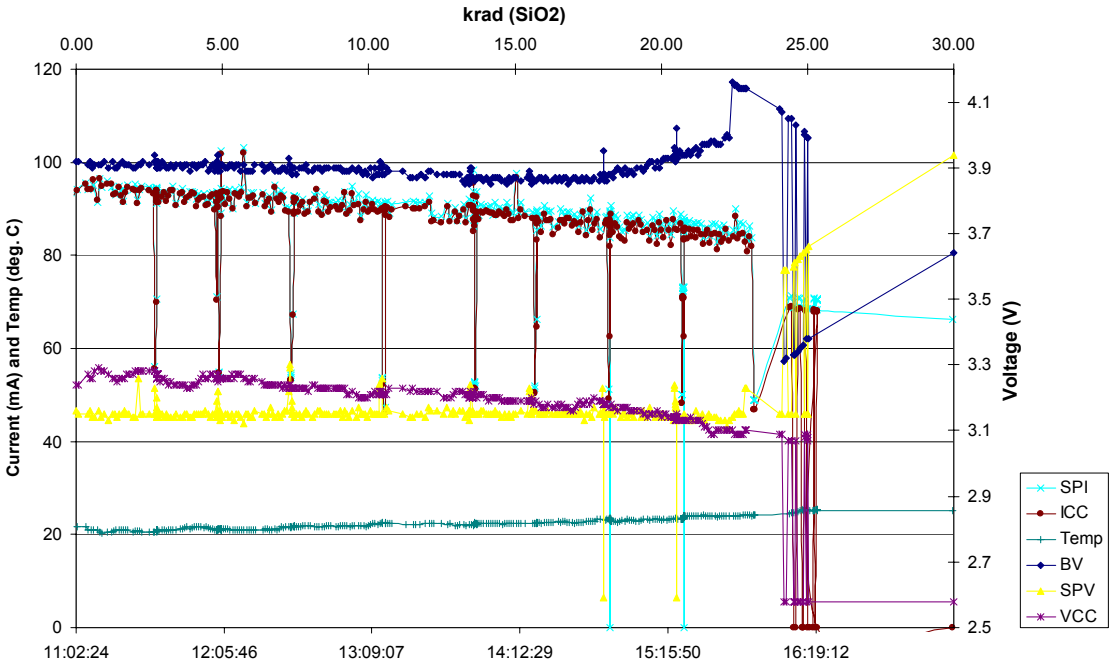

Figure 7-9. Co-60 TID Radiation Results

No measurable effects are observed up to 5 krad (SiO_2). After this point, all six telemetry channels transmitted by the second prototype (battery, solar array, and 3.3 V regulated bus voltage and current) begin to decrease at a very low rate. At 17.5 krads (SiO_2), the test is briefly paused and the chamber is entered to verify the telemetry data by making a measurement with a multimeter. It is found at this point that VCC drops from the original level of 3.3 V down to 3.23 V, which is not unreasonable, but not nominal and explains the slowly falling telemetry values. This quick measurement is repeated at 2.5 krad intervals throughout the remainder of the test.

All systems remain functional through 20 krad (SiO_2) and the total current draw for each prototype remains virtually constant through the end of the test at 30 krad (SiO_2). It was expected that the current would rise throughout the test. The GPS module and real-time clock first exhibit irregular behaviour at 22.5 krad (SiO_2) and both cease functioning by 25 krad (SiO_2), although VCC is still 3.11 V, well above the minimum voltage requirement for each. From 27.5 to 30 krad (SiO_2), VCC drops sharply from 3.05 V to 2.11 V.

Both PCBSats are then more closely examined two hours after completion of the test in the laboratory. It is found that all three ICs of the EPS have degraded in performance, resulting in the overall drop of VCC down to 2.11V at the conclusion of the test. More test points could be measured to find out where each component begins degrading, but the telemetry does indicate that the process starts after 5 krad (SiO_2), where linear voltage regulators are known to fail. Despite this degradation process starting at 5 krad (SiO_2), the system functionality is nearly flawless through 20 krad (SiO_2), which is more than four times the desired hardness level for the mission.

Regarding the first prototype, the ATmega128 operates flawlessly through 30 krad (SiO_2) with no measurable increase in operating current. The ATmega128 on the second prototype operates flawlessly through 27.5 krad (SiO_2), and then behaves erratically due to VCC going below the device threshold. When isolated and powered directly with a nominal 3.3 V, normal operation is restored. The flash memory of both devices is then scanned and verified against the binary file with no discrepancies. The crystal oscillators are also measured and found to remain at the specified frequency; however, the ATmega128's cannot be reprogrammed. This is a well-documented failure mechanism, as the charge pump circuit required for the memory write operation no longer produces the minimum voltage after receiving 8-14 krad (SiO_2) TID [241]. Further investigation is required to determine if the off-chip secondary flash storage is as sensitive.

The DS1302Z real-time clock is isolated and found to have an increased power draw from 200 nA to about 2 mA, which is a 10,000-fold increase. After room temperature annealing, it never regains functionality. The crystal is checked and found to remain at the specified frequency.

The XBee wireless module also performs perfectly through 30 krad (SiO_2) with no measurable increase in operating current. Some wireless telemetry is lost periodically throughout the test, yet considering there is several feet of lead and concrete between the transceivers, this is expected and similarly experienced by other wireless devices being tested at the same time.

Finally, the GPS module is removed and tested independently. It is found to draw only 23 mA when it nominally draws 30 mA. Detailed test data shows that the device operates nominally until a spike in operating current at 22.5 krad (SiO_2), which can be seen in Figure 7-9. After room-temperature annealing it never regains functionality. Table 7-5 gives a summary of the radiation test results by device. Figure 7-9 illustrates a rapid change of telemetry values at the 17.5 krad (SiO_2) point and beyond.

Table 7-5. Summary of Total Ionizing Dose of 30 krad (SiO_2) Response by Device

Device	First Anomaly Point (krad)	Failure Point (krad)	Initial Data	Final Data
ATmega128	none	none*	~4.5 mA	~4.5 mA
XBee	none	none	50 mA	51 mA
iTrax-03S GPS	22.5	25	30 mA	23 mA
DS1302Z	22.5	25	200 nA	2 mA
MAX604	~17.5 krad	~24 krad	3.3V	~2.8 V
MAX856	~17.5 krad	~24 krad	3.3 V	3.18 V
MAX982	~17.5 krad	~24 krad	4.2 V	2.98 V

7.2.6 Thermal-Vacuum Simulation and Testing

The ideal environmental test is a thermal vacuum campaign with integrated AM0 solar illumination. This would truly simulate orbital conditions and expose any weaknesses in the PCBSat thermal design. This type of facility is rare and typically very large, making it an expensive test. Instead, a thermal nodal analysis is performed using ThermXL, which is an ESA-sponsored spreadsheet-based tool for rapid analysis.

The PCBSat thermal environment is specified within the context of a 94.6 minute orbit at a 500 km altitude, where the spacecraft spends 58.9 minutes in the sun and 35.7 minutes in the eclipse. For this average case scenario, the sunlit portion of the orbit gives solar flux G_s of 1360 W·m^{-2}, albedo *alb* of 35%, and Earth infrared q_I of 237 W m^{-2}. The eclipse portion only has an Earth infrared input. A small amount of internal heat dissipation is included and the top and bottom faces are swapped every orbit cycle, simulating a slow attitude roll along the velocity vector.

The thermal model is based on the standard thermal conductivity, density, specific heat, emissivity, and absorptivity values for solar cells, FR4 PCB, and the aluminium shield layer. The satellite is defined by 10×10 cm layers of the appropriate materials and actual thickness. Conduction is defined between the set of solar cells, solar array PCB, and aluminium shield on each side. Radiation occurs between the solar cells and deep space, as well as between the aluminium shields and the core PCB on both sides. Figure 7-10 illustrates the results, noting that the core PCB and battery achieve a steady state temperature of 20 °C after many orbit cycles.

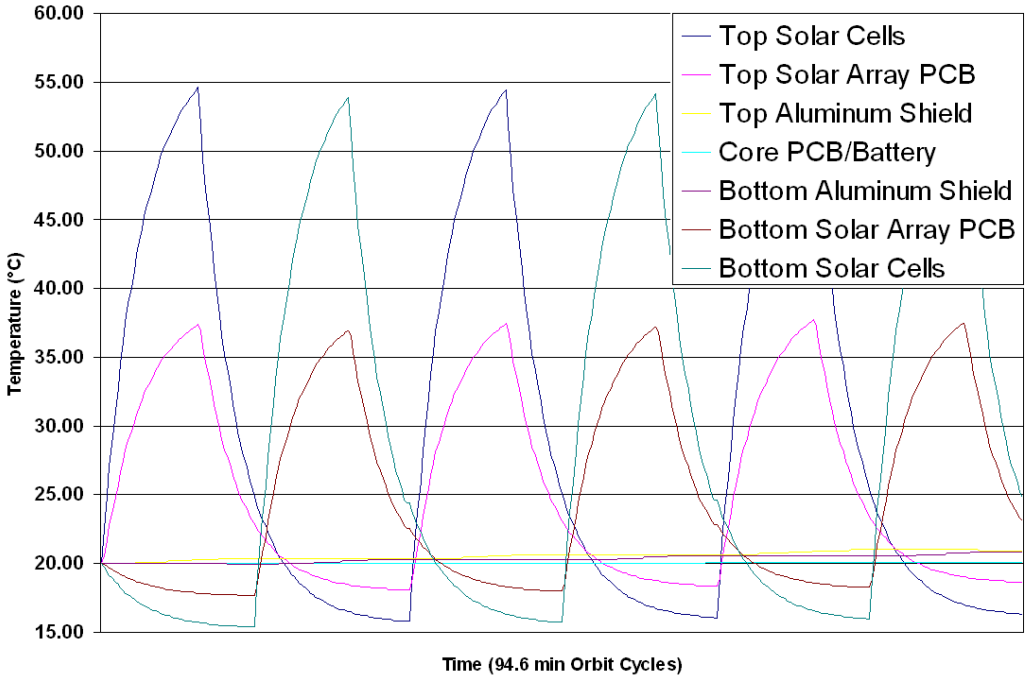

Figure 7-10. PCBSat Thermal Nodal Analysis

At a minimum, a vacuum test is recommended to ensure the viability of certain components, such as the Li-ion battery, as it can bulge or leak in a vacuum depending on the construction. The selected Panasonic battery discussed in Section 6.4 is enclosed in aluminium, but still requires verification. A thermal-vacuum bakeout and thermal-vacuum test is required according to the profiles in Figure 7-11 and Figure 7-12, both at a vacuum of 10^{-5} Torr.

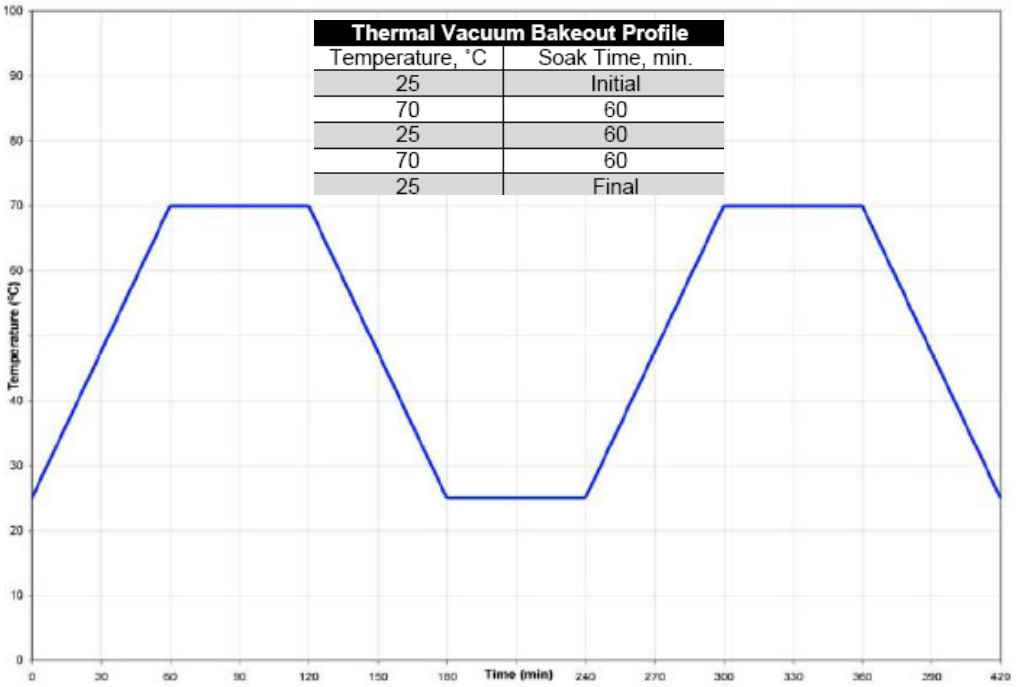

Figure 7-11. Required Thermal Vacuum Bakeout Profile [130]

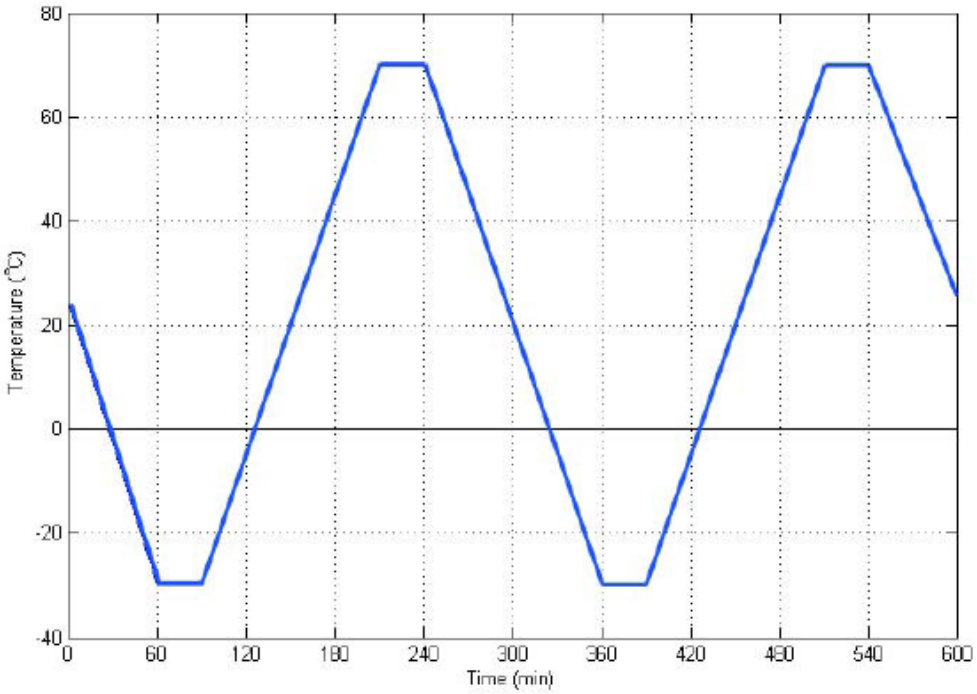

Figure 7-12. Required Thermal Vacuum Profile [130]

7.3 PCBSat Analysis

The final step of the PCBSat investigation is a determination of how well the requirements and constraints, along with the subsequent derived requirements, are met regarding the case study mission presented in Chapter 3. The mission statement and objectives are given in Table 3-2 and top-level quantified mission objectives and constraints in Table 3-3. In summary, they require that plasma density and temperature found in the ionosphere be measured at one sample per second with as many measurement points as practical at a maximum spacing of 100 km between satellites. The target budget is less than $500,000.

The derived system requirements are reported in Table 6-1. They serve to guide the development of the particular PCBSat implementation for the mission. These requirements are now verified in Table 7-6 summarizing the key components and references to performance data reported in Chapter 6 and 7. The primary objective of the case study mission is to demonstrate the utility of a space sensor network based on very small satellites as a low-cost approach to solve a fundamental user-driven mission. This drives the overall top level requirement to use COTS components, processes, and deployment systems. This requirement is met with a few exceptions listed in Table 7-3. Issues with the slight mass overage, Delrin thermal expansion mismatch with aluminium, and environmental testing must be addressed and completed.

The PCBSat design approach is able to accommodate the MESA payload, which is capable of meeting the primary mission requirements of measuring the plasma temperature and density. The power and data requirements are met with the design of the subsystems. A miniaturized radio, GPS module, and GPS antenna are integrated on a core PCB containing the payload, EPS, and DH subsystem components. The core PCB is encapsulated with aluminium plates serving as a thermal buffer and radiation shield. Solar array PCBs are on both outer faces of the satellite, insulated from the core by using a Delrin spacer, which also provides the general structure and launch vehicle interface.

Beyond further environmental analysis and simulation, the only outstanding requirement is to resolve an approach for a space compatible GPS system. Credit card sized systems are available, but are approximately the same size of the XTend radio and use about five times the power of the current GPS hardware.

Table 7-6. PCBSat System Requirements, Configuration, and Performance Data

System	Requirement	Major Result	Reference	Status
Top Level	▪COTS components, processes, deployer	▪Commercial PCBs ▪P-POD	▪Ch. 6 ▪Tab. 7-3	▪Meets ▪Exceptions
Payload	▪Plasma sensor ▪Imager (option)	▪MESA sensor ▪INA121/OPA234U ▪MAX761/765/1247 ▪LTC1664	▪Sec. 3.3.4.4 ▪Sec. 6.3	▪Meets
Orbit	▪Short duration LEO	▪500 km, 30 deg ▪20 krad (SiO_2)	▪Sec. 3.3.4.3 ▪Sec. 7.2.5	▪Meets
Configuration/ Structure	▪P-POD compatibility	▪10×10×2.5 cm ▪311 g ▪FR4/Delrin/Al	▪Sec. 7.1.1	▪Meets
EPS	▪Balanced budget ▪Primary solar power ▪PPT/BCR ▪Regulated 3.3V ▪Power storage ▪Power telemetry ▪RBF/Sep switches	▪+3% margin ▪GaAs/Ge 2×4 cm cells, $\eta \cong 18.8\%$ ▪MAX856/982, 83% ▪MAX604, 92% ▪Panasonic Li-ion +200% margin ▪MAX4072	▪Sec. 6.4 ▪Sec. 7.2.2 ▪Sec. 7.1 ▪Sec. 7.1 ▪Sec. 6.4 ▪Sec. 6.4 ▪Sec. 6.4	▪Meets
DH	▪3.3V RISC CPU ▪128K flash for code ▪16Mb flash for data	▪Atmel Mega128L 7.6 MHz ▪15% used ▪6% used/eclipse	▪Sec. 6.5 ▪Sec. 3.3.4.3	▪Meets
Comm	▪Unlicensed band ▪Mesh network ▪100 km range	▪MaxStream XTend 900 MHz ISM 9600 bps, 500 mW MeshX ▪147 km range	▪Sec. 6.6	▪Meets
AOCS	▪Orbit determination ▪Ram attitude control	▪iTrax-03S GPS ▪Sarantel Geo-SMP ▪Mass offset/drag tail	▪Sec. 6.7	▪Exception
Propulsion	▪None			
Thermal	▪Pass. thermal control ▪2-channel telemetry	▪Al plates ▪Thermistor	▪Sec. 6.8	▪TBD

7.4 Summary

A complete discussion of the required functional and environmental tests is given regarding the suitability of using the PCBSat miniaturisation approach to meet the case study mission requirements set forth in Chapter 3. Two exceptions arise regarding the P-POD deployer and the GPS receiver. However, these issues are not insurmountable and can be address with further investigation. More environmental testing is required when the opportunity presents itself. Overall, nearly all of the primary and derived mission requirements are met, demonstrating that the PCBSat approach can be used to design a very small satellite that can perform a useful mission.

Chapter 8

8 Cost Effectiveness of Very Small Satellites

Five key technologies are considered in this research and compared for cost-effectiveness by evaluating their cost against power generation and payload volume metrics along with case study mission suitability. Section 8.1 presents the motivation for assessing the cost-effectiveness of these technologies. Section 8.2 details the cost and performance derivations for each technology. The results of this component of research are graphically illustrated in Section 8.3.

8.1 Introduction

The real measure of value for a small satellite in a distributed space mission is the utility of the system. Demand for such missions is less sensitive to cost than is widely thought, but is first order sensitive to the value of the product delivered. This explains why ~100 kg microsatellites have proliferated in the small satellite market, instead of much smaller satellites, despite the lower unit cost of the latter [112]. However, for certain missions where a large number of in-situ measurement points is a mission requirement, a very small, low cost solution is essential, provided that a sufficient but small enough payload and bus solution exists.

A review of the very small satellite technologies investigated in this research is presented in Figure 8-1. Traditional picosatellites, bolstered by the CubeSat community, have risen to a place of prominence. Twenty three picosatellites have flown since 2000, where 17 of them have conformed to the CubeSat standard. In most cases, these efforts are educational activities.

Microengineering of aerospace systems is the pursuit of a variety of satellite miniaturisation techniques focusing on microfabrication and micromachining, in addition to suggesting that multifunctional structures can further enhance miniaturisation. However, this approach remains expensive and not yet applicable, as discussed further in this chapter.

Two technologies are developed in this research based on reviving previously proposed concepts. SpaceChip captures our imagination of what might be possible in terms of the ultimate in satellite miniaturisation. The focus is on monolithic integration of all satellite functionality on a single commercially produced CMOS chip. The available power, payload selection, and communication range prove to be the greatest limiting factors, so the technology is recommended for sensor network applications in hostile environments where the separations are sufficiently short.

PCBSat takes a different approach, investigating what is possible using commercial components and common fabrication practices. PCBSat is able to achieve the goals of SpaceChip, by delivering a cost-effective solution based on commercial parts and manufacturing practices. A final configuration of 10×10×2.5 cm, 311 grams is reached, which integrates nearly all typical satellite functions, except propulsion, using a novel approach.

A hybrid of SpaceChip and PCBSat is briefly introduced in this section as an undeveloped concept, to investigate whether MCM technology might be a more cost-effective approach for assembly of an entire satellite, dubbed MCMSat. Similar to microengineered aerospace systems, MCM integration has a debatable return on investment, as the costs are significantly higher.

All of these technologies now become more relevant in a space sensor network context. To compare these technologies, the case study mission presented in Chapter 3 is used to set the baseline requirements and provide a basis for comparison. The plasma bubble mission is intended to represent a family of space sensor network missions enabled by very small satellites.

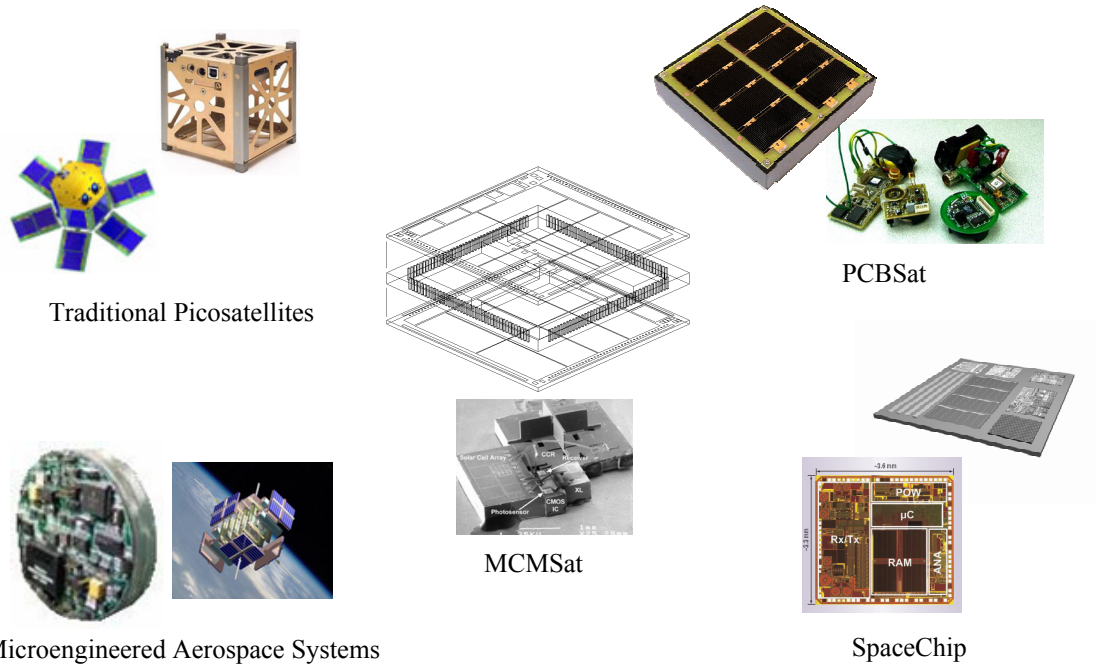

Figure 8-1. Review of Spacecraft Miniaturisation Technologies

8.2 Technology Cost and Performance Derivations

This chapter is not intended to be an exhaustive and authentic cost modelling process. Still, great care is taken to obtain the most reliable cost estimates as possible and fairly estimate any missing data points. Much of the data has been obtained directly from the vendors. In some cases, vendors are willing to envisage costs for hundreds to tens of thousands of units. Cost modelling assumptions are defined in determining all technology costs as listed in Table 8-1.

Table 8-1. Cost Modelling Assumptions

- Maximum attainable performance parameters shall be used
- Maximum size shall be limited by technology or 10×10×10 cm and 1 kg
- Launch costs shall be standardised to historical Dnepr data
- Non-recurring engineering (NRE) shall not be included
- Assembly, integration, and test (AIT) shall not be used, unless needed to equate systems

In order to determine a cost versus performance relationship for comparison, ideally, key performance metrics should be properly identified. Two logical parameters are sunlit average power generation and payload accommodation. Most other system capabilities, such as payload support, on-board computing, communication range, can be determined from these and the assumptions listed above. For all scenarios, a single COTS OSCAR-class ground station is assumed and can be installed for approximately $50K [242].

8.2.1 COTS CubeSat Cost and Performance

The notion of a COTS CubeSat has been introduced recently [73], but no cost estimates have been discussed in detail other than in [112]. In the case of mass-producing CubeSats, all the vendors have been enthusiastic about providing approximate, non-binding costs for massively distributed mission scenarios. Regarding the case of the MESA payload, GPS receiver, and launch costs, these are estimated by the author by using an extrapolation based on the average of the break point reductions. The baseline CubeSat radio is the Microhard MHX-2400; however, the Digi XTend is preferred, as discussed in Section 6.6. For a relay satellite configuration, required for all scenarios, the ISIS UHF/VHF radio is used in place of the MESA payload [242]. The COTS CubeSat is estimated to have an average sunlit power generation of 2.4 W [221] with triple-junction cells and has an approximate payload capacity of 300 g and 9×9.5×3cm (actual).

Table 8-2. COTS CubeSat Configuration and Costs

*approximate non-binding costs from vendors **extrapolated cost by author

Subsystem	Vendor		Model	Mass (g)	Unit Cost @1	Unit Cost @1000
Payload	USAFA	[243]	MESA	130	$2,763*	$1,517**
Structure	Pumpkin	[244]	Skeletonized	155	$1,350*	$810*
EPS	Clyde Space	[245]	CubeSat EPS	310	$25,240*	$19,252*
DH	Pumpkin	[244]	FM430	90	$1,200*	$720*
Comm	Digi	[246]	XTend	18	$179*	$90*
ADCS	-		bar magnet	25	-	-
GPS	SSTL	[247]	SGR-05	20	$20,000*	$6,000**
Propulsion	none		-	-	-	-
Launch	CubeSat	[248]	Dnepr	-	$40,000*	$20,000**
TOTALS:				**748**	**$90,732**	**$48,389**
Comm	ISIS	[242]	UHF/VHF	120	$25,600*	$15,360**
TOTALS:				**738**	**$116,332**	**$63,749**

8.2.2 Microengineered Aerospace Systems Cost and Performance

Although microengineered aerospace systems initially explored a variety of miniaturisation techniques for satellites as discussed in Section 2.3.2.1, their recent focus is on very small satellite propulsion systems. For example, the one-kilogram COSA is an investigation into a weeklong satellite self-inspection mission. The propulsion system under development has demonstrated a ΔV capability of 30 m/s [86]. Start-up costs are initially estimated at $600,000 with a unit cost of $30,000 for the structural/propulsion subsystem alone [249]. A battery and conventional PCB provide the payload and subsystem functionality for the demonstrator.

Since COSA is primarily focused on a propulsion system for spacecraft inspection, it would not be fair to compare this technology in a mission scenario where propulsion is not required or desired, therefore, it is not included in this comparison. It should be noted that this promising technology is well suited for a complete propulsion system for picosatellites, which currently does not exist. Not enough information about other similar approaches discussed in Section 2.3.2.1 is available to make any kind of comparison.

8.2.3 SpaceChip Cost and Performance

SpaceChip costs are simply based on manufacturing costs of low-end CMOS wafers, such as 0.35 μm technologies, including SiGe BiCMOS. Currently, these costs are generically at $120,000 for an engineering run, which includes masks and two 200 mm wafers, each able to hold 40-50 reticle-sized designs. Production wafers cost $6,000 each with a minimum quantity of 25 [250].

The main advantage of this approach is a complete turnkey solution, where the spacecraft design is sent electronically to the foundry for mass production. Recall that to meet various basic system requirements, two die must be sandwiched on a thermal substrate, with an assumed minimal cost. With a 20×20×3 mm, 10 g configuration, a maximum of 2,500 SpaceChips could be deployed from one 2.5 kg P-POD and would have a total mass of 27.5 kg. SpaceChip's costs are highlighted in Table 8-3. SpaceChip cannot meet the mission requirements set out in the Chapter 3 case study. It is still included in the cost versus performance analysis. SpaceChip has an average sunlit power generation of 1 mW whilst the payload capacity is negligible.

Table 8-3. SpaceChip Configuration and Costs

*approximate non-binding costs from vendors **extrapolated cost by author

Item	Vendor/ Model	Mass (g)	Unit Cost @1*	Unit Cost @1,000
SpaceChip	Various [250]	10	$2,400*	$400*
Launch	CubeSat [248]	-	$300**	$300**
TOTALS:	**-**	**-**	**$2,700**	**$700**

8.2.4 PCBSat Cost and Performance

The costs for PCBSat are determined at the piece-part level, summarized in Table 8-4 and detailed in Figure B-2, p. 206. As most of the parts are typically ordered in large quantities, it is relatively straightforward to determine accurate costs at higher numbers. PCB labour costs are included in the component costs to equate the pricing to the assembled module level. Note that the solar cell cost includes flight preparations to bare cells, doubling the cost. One debatable point of the PCBSat cost is the GPS receiver, as in its current configuration, it will not function in space as discussed in Section 7.2.4 without firmware modification. The average sunlit power generation for PCBSat is 880 mW (triple-junction cells) and the available payload capacity is 5×5×0.5 cm. As with COTS CubeSat, all mission requirements can be met, but at lower performance levels.

Table 8-4. PCBSat Configuration and Costs

*approximate non-binding costs from vendors **extrapolated cost by author

Item	Vendor/ Model	Mass (g)	Unit Cost @1	Unit Cost @1,000
Payload	USAFA/MESA [243]	33.3	$2,703**	$1,493**
Structure	various	145	$80*	$48**
Components	various	13	$395*	$191*
Solar Cells	various	92.1	$1,600*	$960**
Comm	Digi/XTend [246]	27.4	$179	$90
Launch	P-POD [248]	-	$8,000	$6,000
TOTALS:	**-**	**311**	**$12,957**	**$8,782**

8.2.5 MCMSat Cost and Performance

MCM technology has been used for some time to miniaturize satellite components. Building on that idea, the satellite-on-a-MCM concept, a hybrid of SpaceChip and PCBSat, would implement an entire satellite using one or more MCM substrates. Working under the same assumptions and constraints, the average sunlit power generation also drives the MCMSat configuration requiring the same area for solar cells. We are then led to the same 10×10 cm configuration to maintain compatibility with the P-POD deployer. The advantage that MCM encapsulation offers is a reduction in thickness and mass.

MCM-L (chip-on-board) is briefly examined, but at the one kilogram scale, does not offer much of an advantage over traditional PCBs, as it does not allow embedding of components in multiple layers. Whilst MCM-C (ceramic) and MCM-D (thin-film) approaches are considered viable; this simple study focuses on MCM-D due to its higher compactness and flexibility. Two assumptions are made to derive the MCMSat cost using MCM-D. First, it is assumed that all ICs being used in PCBSat are available as bare die. Secondly, the component type, count, cost, and interconnectivity is assumed to be the same as PCBSat. This leads to an approximate thickness of one centimetre [112].

Construction is based on a patterned overlay technology, which allows extremely close component placement (< 0.5 mm) of ICs whilst forming a flat, chip-like surface. MCMSat is composed as a stack of three MCMs, interconnected through a 2 mm, 80-contact border array between substrates as shown in Figure 8-2. The RF subsystem is formed using four, 1.5×82 mm crossed dipoles, and the power subsystem employs eight, 20×40 mm GaAs solar cells as shown in Figure 8-3 (left). Traditional microelectronics components are strategically placed on the substrates. All components are recessed within the substrates. This arrangement permits the surface attachment of other components (including payload). Payload components can be placed on each layer [112].

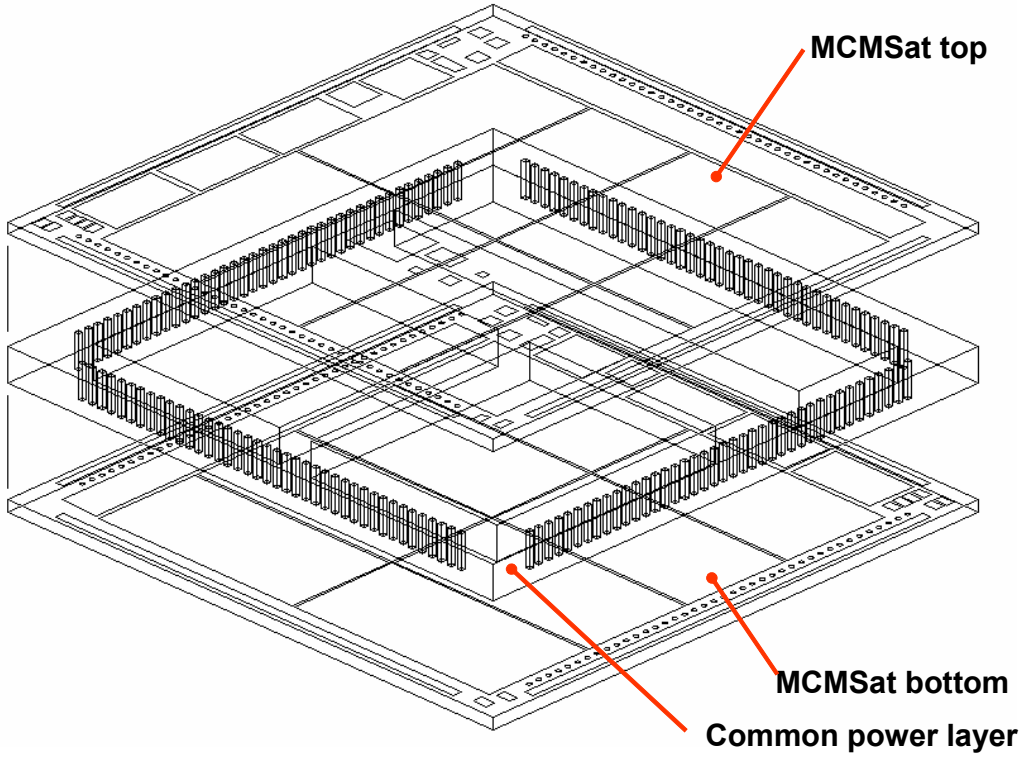

Figure 8-2. MCMSat Notional Configuration [112]

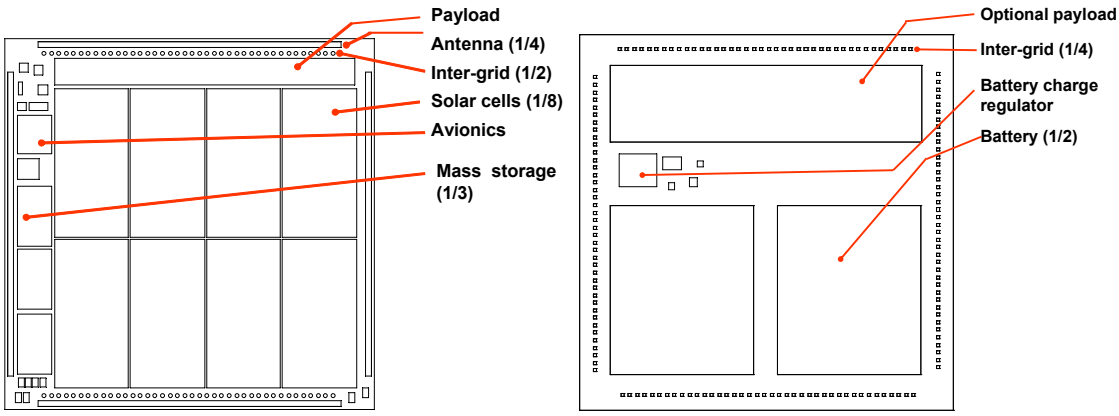

Figure 8-3. MCMSat Top (left) and Bottom (right) Layers [112]

MCMSat is essentially similar to PCBSat, with the centre layer sandwiched by outer solar cell substrates. The centre layer-substrate is dedicated to power storage, supporting two 35×45×5.5 mm batteries, uniformly distributed to each substrate through internal battery charge regulation circuitry. An estimated cost of \$50/cm^2/layer is used to support the cost estimate [251]. An internal bay is available for additional payload (2×8×0.6 cm). Based on these assumptions, approximate costs are shown in Table 8-5.

Table 8-5. MCMSat Configuration and Costs

*approximate non-binding costs from vendors **extrapolated cost by author

Item	Vendor/ Model	Mass (g)	Unit Cost @1	Unit Cost @1,000
Payload	USAFA/MESA [243]	80	\$2,703**	\$1,493**
Structure	various	40	\$15,069*	\$9,041**
Components	various	50	\$534*	\$231*
Solar Cells	various	-	\$1,600*	\$960**
Launch	P-POD [248]	-	\$4,000*	\$3,000**
TOTALS:	**-**	**170**	**\$23,906**	**\$14,725**

The sunlit average power generation for MCMSat is identical to PCBSat at 880 mW. The available payload capacity is smaller than PCBSat at 1×8×0.2 cm on two faces, with an additional 2×8×0.6 cm inside. As with PCBSat, all mission requirements can be met.

8.3 Satellite Cost and Performance Comparison

A detailed breakdown of costs at the 1, 10, 100, 1000, and 10,000 satellite quantity levels is given in Table 8-7 at the end of this Chapter and is used to generate the figures in this section. Comparing preliminary results of the four technologies considered reveals some interesting results. As expected, SpaceChip has the lowest unit cost as shown in Figure 8-4.

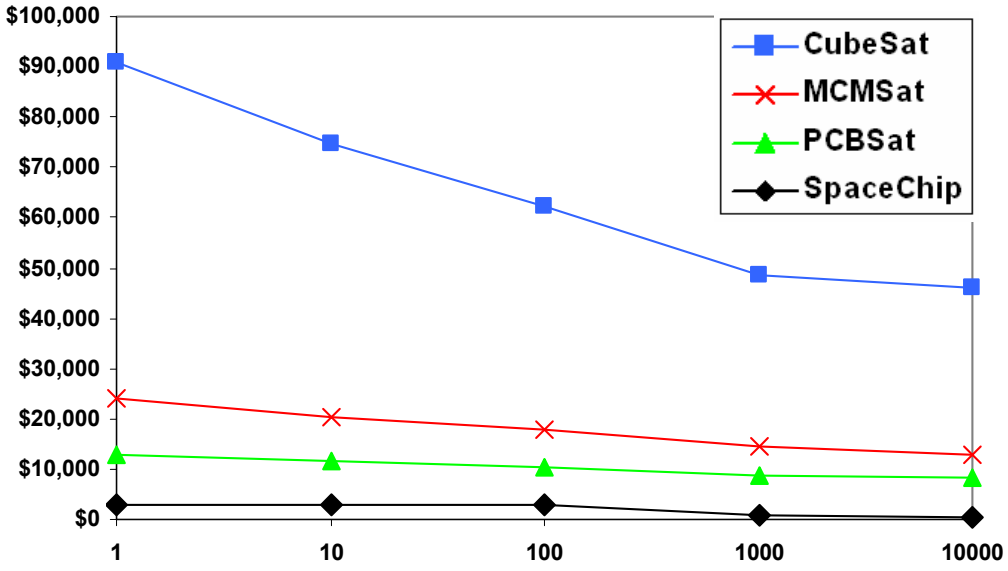

Figure 8-4. Unit Cost vs. Constellation Size

Unit cost can be irrelevant without a performance metric, such as average sunlit power generation as shown in Figure 8-5. In this case, SpaceChip is cost-prohibitive at $550,800/W (off the chart), with a constellation size of 10,000. PCBSat proves to be the most cost effective at any quantity.

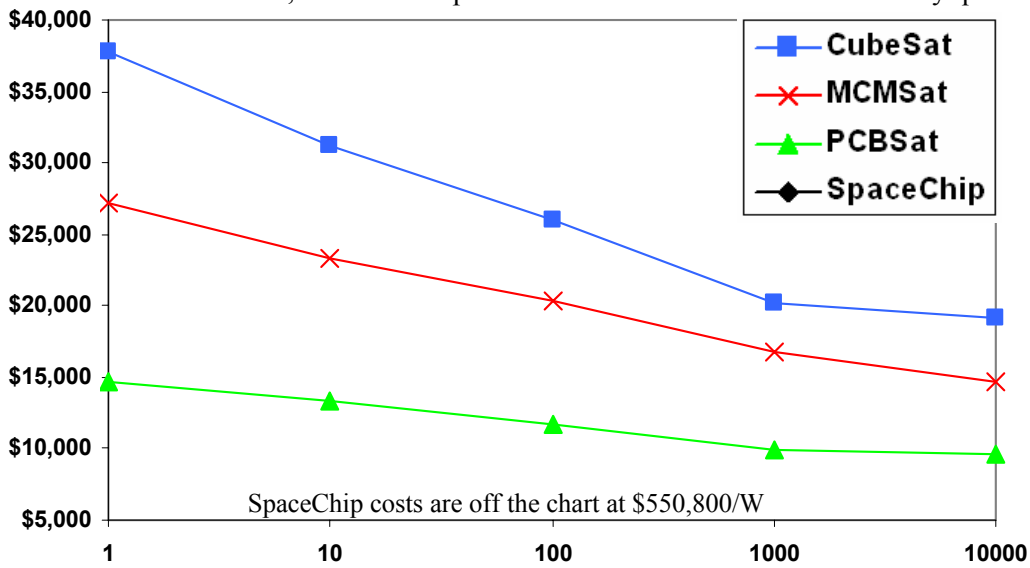

Figure 8-5. Cost/Watt vs. Constellation Size

Looking at the cost of payload volume shown in Figure 8-6, CubeSat emerges as the most cost effective, when the maximum available payload volume is considered. SpaceChip is again off the chart at $22M per cm^3 for a constellation size of 10,000.

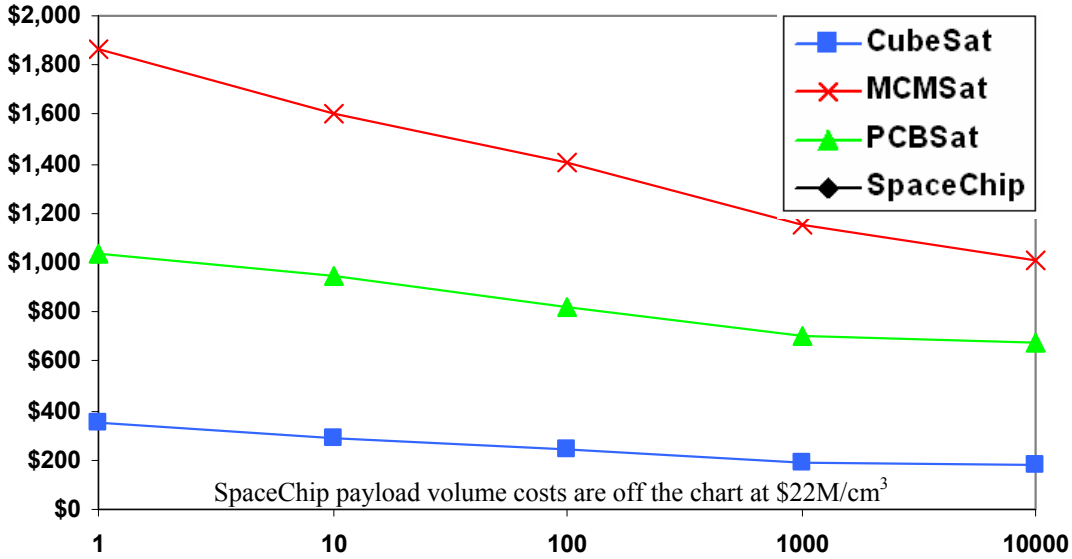

Figure 8-6. Cost/Maximum Payload Volume (cm^3) vs. Constellation Size

A comparison of entire constellation costs is shown in Figure 8-7; however, this figure does not include the required relay satellite cost. The ratio of required relay satellites is given in Table 8-6 and is based on including one relay satellite in each P-POD, with the exception of an all-CubeSat constellation, where the ratio is appropriately set. In the all-CubeSat constellation, the challenge of unmaintained constellations with multiple deployments is not yet addressed. Figure 8-8 is the revised result including the relay satellites at the appropriate ratio in the entire constellation costs.

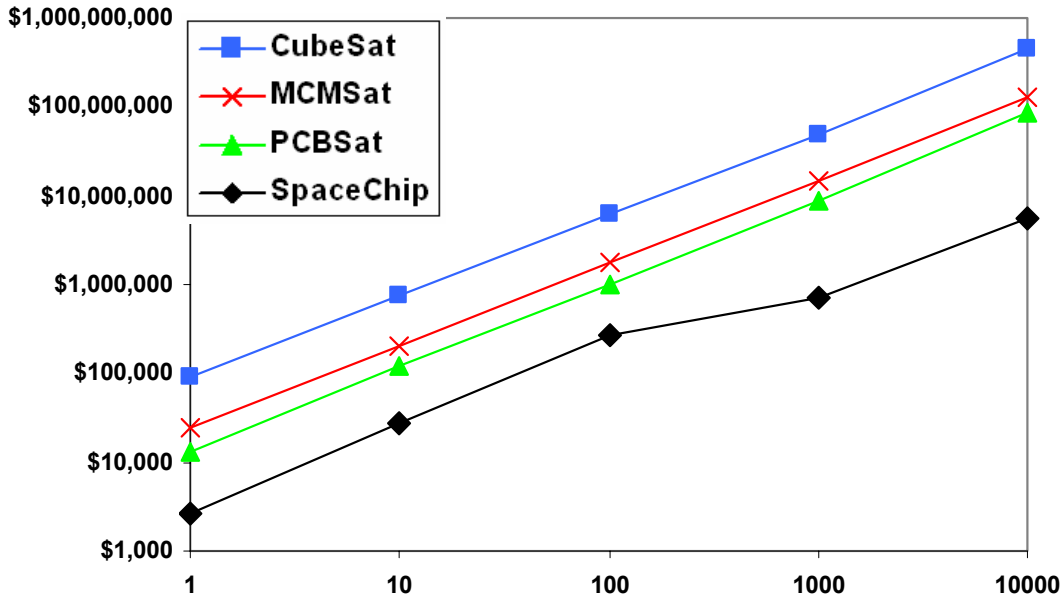

Figure 8-7. Entire Constellation Cost Without Relay Satellite (y log scale)

Table 8-6. Ratio of Relay Satellites

Technology	Relays per P-POD	Remaining Satellites per P-POD	Satellites per Relay
CubeSat	1:4	11:4	12:1
SpaceChip	1:1	1667	1667:1
PCBSat	1:1	8	8:1
MCMSat	1:1	20	20:1

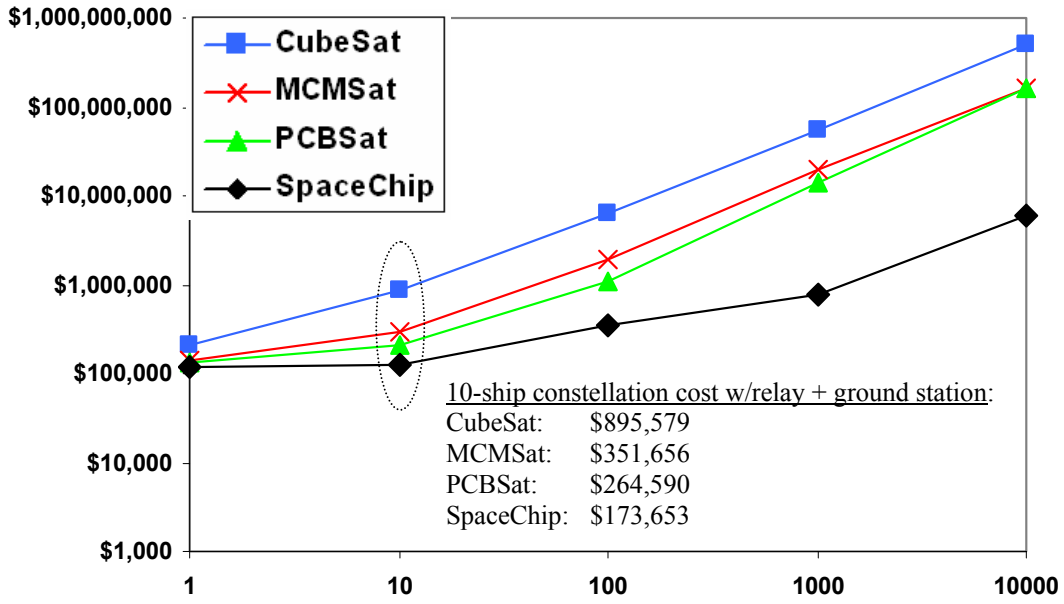

Figure 8-8. Entire Constellation Cost With Relay Satellites (y log scale)

Finally, Figure 8-9 compares single unit costs of the technologies presented here with SSTL's range of microsatellite buses. Similarly, Figure 8-10 and Figure 8-11 compare cost per watt and cost per cubic centimetre of payload. Note that costs denoted by SSTL* are approximated by the author based on the best available public information [252].

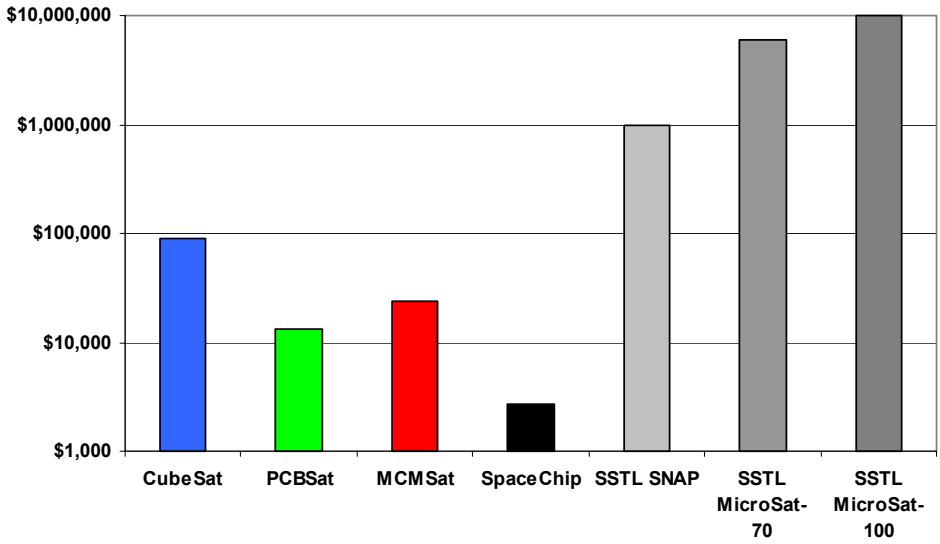

Figure 8-9. Unit Cost Comparison with SSTL Buses (y log scale)

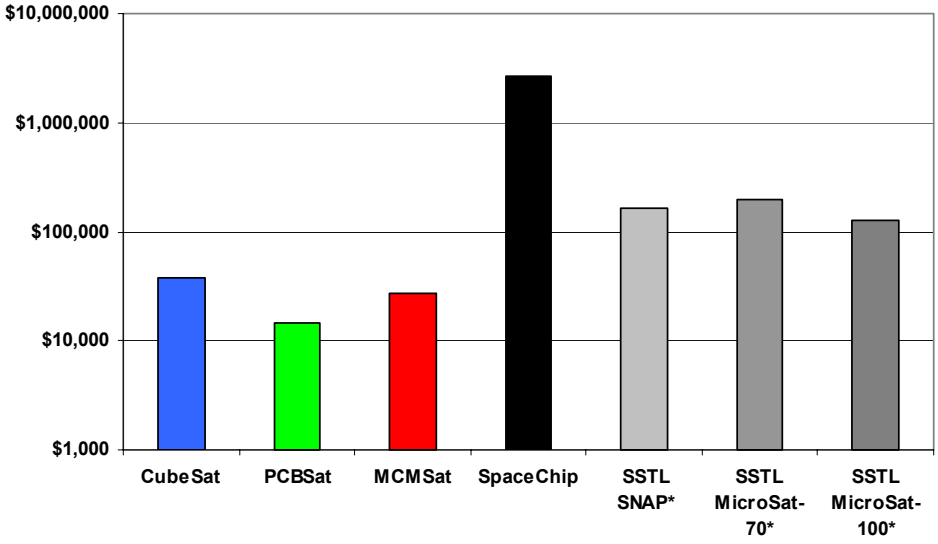

Figure 8-10. Cost/Watt Comparison with SSTL Buses (y log scale)

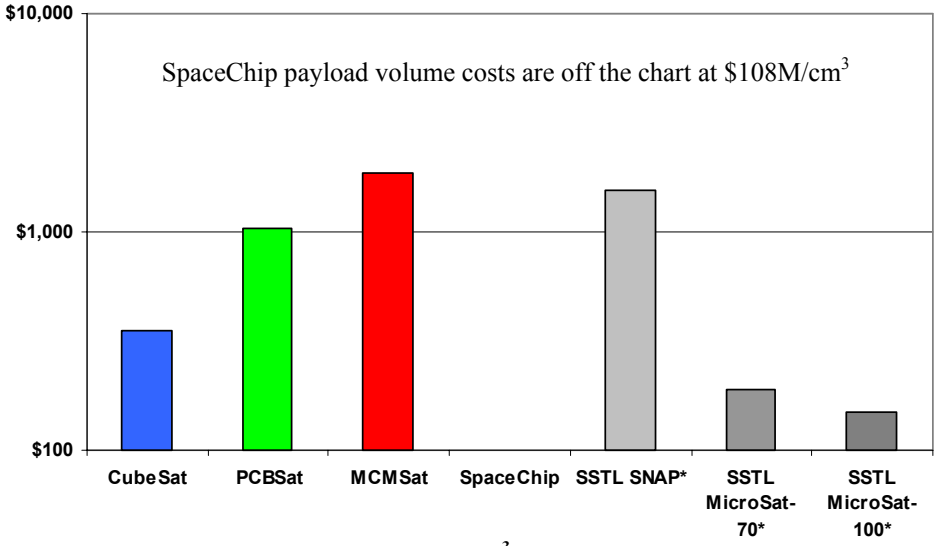

Figure 8-11. Cost/Max Payload Volume (cm^3) Comparison with SSTL Buses (y log scale)

Table 8-7. Detailed Cost Breakdown of All Technologies

	Component	Vendor	Mass	1	10	100	1,000	10,000														
				Cost	Cost	Cost	Cost	Cost														
CubeSat	Payload	MESA	80	$2,600	$1,800	$1,600	$1,450	$1,300	1	$2,600	10	$1,800	100	$1,600	1000	$1,450	10000	$1,300				
	Interface PCB	various	50	$123	$92	$54	$43	$41														
	PCB Labor	Aspen	-	$40	$34	$30	$24	$20	1	$40	5	$34	25	$30	500	$24	5000	$20				
	Structure	CubeSat Kit	155	$1,350	$1,148	$1,013	$810	$675	1	$1,350	5	$1,148	25	$1,013	500	$810	5000	$675				
	EPS	Clyde Space	310	$25,240	$22,120	$20,618	$19,252	$18,305	1	$25,240	10	$22,120	100	$20,618	1000	$19,252	10000	$18,305				
	DH	CubeSat Kit	90	$1,200	$1,020	$900	$720	$600	1	$1,200	5	$1,020	25	$900	500	$720	5000	$600				
	Comm	Maxstream	18	$179	$179	$120	$90	$90	1	$179	25	$149	100	$120	1000	$90	1.00E+12	$999				
	GPS	SSTL	20	$20,000	$13,500	$8,000	$6,000	$5,000	1	$20,000	10	$13,500	100	$8,000	1000	$6,000	10000	$5,000				
	ADCS	(bar magnet)	25	$0	$0	$0	$0	$0		$0												
	Thermal	(passive)	0	$0	$0	$0	$0	$0		$0												
	Launch			$40,000	$35,000	$30,000	$20,000	$20,000	1	$40,000	10	$35,000	100	$30,000	1000	$20,000	1.00E+12	$999				
			748	**$90,732**	**$74,893**	**$62,335**	**$48,389**	**$46,031**														
				$25,600	$21,760	$19,200	$15,360	$12,800		$25,600	5	$21,760	25	$19,200	500	$15,360	5000	$12,800				
				$116,332	$96,653	$81,535	$63,749	$58,831														
PCBSat	Payload	MESA	80	$2,600	$1,800	$1,600	$1,450	$1,300	1	$2,600	10	$1,800	100	$1,600	1000	$1,450	10000	$1,300				
	Payload components	various	50	$103	$100	$54	$43	$41														
	Bus PCB & components	various	70	$355	$252	$178	$141	$140														
	PCB Labor	Aspen	-	$40	$34	$60	$51	$51	1	$40	5	$34	25	$30	500	$24	5000	$20				
	Solar cells	EMCORE		$1,600	$1,360	$1,200	$960	$800		$1,600	5	$1,360	25	$1,200	500	$960	5000	$800				
	Structure	various	41	$80	$68	$60	$48	$40	1	$80	5	$68	25	$60	500	$48	5000	$40				
	Xtend	Maxstream	18	$179	$179	$120	$90	$90	1	$179	25	$149	100	$120	1000	$90	1.00E+12	$999				
	Launch			$8,000	$8,000	$7,000	$6,000	$6,000	1	$8,000	10	$8,000	100	$7,000	1000	$6,000	1.00E+12	$999				
			259	**$12,957**	**$11,794**	**$10,272**	**$8,782**	**$8,462**														
MCMSat	Payload	MESA	80	$2,600	$1,800	$1,600	$1,450	$1,300	1	$2,600	10	$1,800	100	$1,600	1000	$1,450	10000	$1,300				
	Interface Parts	various	30	$103	$100	$54	$43	$41														
	Subsystem Parts	various	20	$355	$252	$178	$141	$140														
	Solar cells	EMCORE		$1,600	$1,360	$1,200	$960	$800		$1,600	5	$1,360	25	$1,200	500	$960	5000	$800				
	Structure	various	40	$15,069	$12,809	$11,302	$9,041	$7,535	1	$15,069	5	$12,809	25	$11,302	500	$9,041	5000	$7,535				
	Xtend	Maxstream		$179	$179	$120	$90	$90	1	$179	25	$149	100	$120	1000	$90	1.00E+12	$999				
	Launch			$4,000	$4,000	$3,500	$3,000	$3,000	1	$4,000	10	$4,000	100	$3,500	1000	$3,000	1.00E+12	$999				
			170	**$23,906**	**$20,500**	**$17,954**	**$14,725**	**$12,906**														
SpaceChip	SpaceChip		10	$2,400	$2,400	$2,400	$400	$251	1	$2,400	50	$2,400	675	$400	10000	$251	1.00E+12	$999				
	Launch			$300	$300	$300	$300	$300	1	$300	100	$300	1000	$300	10000	$300	1.00E+12	$999				
			10	**$2,700**	**$2,700**	**$2,700**	**$700**	**$551**														

8.4 Summary

An initial cost model is presented for all technologies discussed in this research: CubeSat, microengineered aerospace systems, PCBSat, and SpaceChip. MCMSat is briefly introduced as a hybrid concept between PCBSat and SpaceChip. These technologies are also compared to more established nano and microsatellite busses of the small satellite industry. Unit costs, cost per watt, and cost per payload volume are the chosen metrics. The suitability of all technologies is briefly discussed regarding the case study mission, set out in Chapter 3.

The CubeSat platform can clearly satisfy the case study mission requirements. CubeSat is more expensive than PCBSat and MCMSat in terms of unit costs and cost per watt, but is the clear leader for the payload volume metric, where it is the least expensive. Microengineered aerospace systems cannot be fairly included in the cost comparison, as this advanced technology is currently focused on the structural and propulsion subsystems in addition to multifunctional structures. SpaceChip clearly has the lowest unit costs, yet is the most expensive of any technology in terms of the chosen metrics. PCBSat comes in second in unit costs, has a clear advantage in terms of cost per watt, but loses out to CubeSat in terms of payload volume. Finally, the hybrid concept of MCMSat ranks just below PCBSat in all cases.

Complete case study mission costs are also discussed, including the required baseline CubeSat relay satellite at the appropriate ratio. The pricing structure does not change, as CubeSat is the most expensive, followed by MCMSat, PCBSat, then SpaceChip. All technologies are significantly below the case study mission goal budget of $500,000, except CubeSat, with a total cost of $895,579, which includes the ground station. PCBSat total costs are $264,590 and MCMSat total costs are $351,656. All of these technologies can meet the minimum requirements of the case study mission. It is possible to deploy a constellation of 1,667 SpaceChips with a relay satellite at a cost of $173,653; however, this technology cannot satisfy the minimum mission requirements.

Finally, all technologies are compared at the single unit cost level with established small satellite buses. An interesting result is that all sub-kilogram technologies considered in this research are at least an order of magnitude cheaper in terms of unit cost and cost per watt. However, cost of payload volume is within the same order. Additionally, non-recurring engineering costs are not included in this investigation, whilst the established system costs include these costs.

Chapter 9

9 Conclusions

This chapter summarizes the concepts and results presented in this research. Firstly, the summaries from each chapter are briefly reviewed in Section 9.1. The aims and objectives proposed for this research are revisited and assessed in Section 9.2. Then, major contributions to the state of the art are discussed in Section 9.3 specifically in terms of the novelty of the work. Section 9.4 concludes the chapter with a brief discussion on the way forward for future research.

9.1 Review of Summaries

Chapter 2 presents the motivation for this work, highlighting that with increasing frequency, new missions are being put forth that require the massive distribution of satellites. Previously, formation flying received most of the academic attention, with little regard to the development of enabling cost-effective miniaturized space systems. More recently, new concepts, such as spacecraft fractionation, have re-emphasized the potential application space and the need for supporting technologies in the context of making multipoint remote sensing or in-situ observations. In parallel, terrestrial wireless sensor networks are flourishing, developing the required wireless networking architectures.

Chapter 3 presents and initially assesses a meaningful user-driven science mission discussed among the many introduced in Chapter 2. The selected case study mission focuses on ionospheric plasma depletions, known as plasma bubbles, believed to be a major source of satellite communication and navigation signal outages, particularly in equatorial regions, during the period after local sunset. A thousand to one disparity in terrestrial versus space weather sensors is exacerbated by rare single-point multi-million dollar satellites, which examine this problem as a secondary or tertiary mission, with the exception of the recently launched C/NOFS mission. A massively distributed mission conducting three-dimensional in-situ measurements is required to demystify this phenomenon.

Basic requirements are developed for an initial constellation of ten satellites, although eight are ultimately used with an unprecedented low cost mission goal of under $500,000. Initial simulations suggest that an entire constellation can deploy from a COTS launch vehicle and deployer, relying on atmospheric drag and solar radiation pressure to naturally distribute the

constellation. Measurements are then taken during the eclipse, using a miniature plasma sensor whose data is time and position stamped by GPS. A co-orbiting, ballistic coefficient matched master relay satellite will poll each satellite in the constellation using an ad-hoc multi-hop mesh network during the sunlit portion of the orbit. The master relay satellite then transmits the measurement campaign data to an amateur-class ground station.

Chapter 4 presents the SpaceChip monolithic SoC approach to fabricate large numbers of wireless sensor nodes for hostile environments including space. A feasibility study is presented, featuring a generalized system architecture composed of a payload sensor and supporting subsystems implemented in SiGe BiCMOS. Chip-scale sensors are proliferating based on CMOS and emerging CMOS–MEMS technologies, although the small size of SpaceChip can be the primary limiter for some payloads. Micro-power generation and storage options are the key enablers for self-powered wireless sensor networks, yet very little advancement has taken place. Data handling is a straightforward application in CMOS, but environmental tolerance must be considered. Similarly, SoC radios with integrated data processing are now commonplace with a range up to one kilometre using external components and antennas, as integrated antennas only have a range of a few metres. SoC GPS is needed for position determination, but they require external components and require too much power. If attitude and orbit control are required, integrated sensors and actuators are possible, but not yet practical. Finally, thermal control is relatively straightforward, with the application of passive thermal control substrates and asynchronous logic.

Overall, payload volume, power generation, and communication range prove to be the most limiting aspects of the SpaceChip approach. These limitations strongly suggest that the concept of SpaceChip is most suited to wireless sensor network applications in hostile environments where the communication range is sufficiently short.

Chapter 5 introduces two essential building blocks for heterogeneous SoC sensor nodes. A novel technique is discovered for monolithically integrating solar cells in SiGe BiCMOS, which can be connected in series to achieve required chip-level operating voltages. This development is widely applicable to a rapidly growing number of SoC devices. Secondly, the application of radiation hardening by design to asynchronous logic is suggested as a unique approach for bare die SoC implementations in hostile environments. A case study is presented using a common design indicating the approach is well suited for applications in radiation and thermal extremes.

Chapter 6 presents the PCBSat satellite miniaturisation approach, which is focused on determining the smallest practical satellite within the context of space sensor networks. PCBSat is based on a satellite-on-a-PCB, representing the strategy of constraining the satellite systems engineering process to using COTS components, fabrication processes, and deployment systems. A flight model prototype is designed and built, targeting application to the Chapter 3 case study

mission to demonstrate the merit of this approach. PCBSat is applicable to a wide range of missions beyond the case study.

Chapter 7 details the functional and environmental tests and results to verify that the PCBSat design approach can meet the mission requirements set forth in the case study. The only significant complication is the licensing requirements for modification of the GPS module firmware. Ultimately, PCBSat demonstrates that it is a novel approach to satellite miniaturisation.

Chapter 8 presents an initial cost model for all technologies discussed in this research: CubeSat, microengineered aerospace systems, PCBSat, and SpaceChip. MCMSat is briefly introduced as a hybrid concept between PCBSat and SpaceChip. Finally, these technologies are compared to more established nano and microsatellite busses of the small satellite industry. Unit costs, cost per watt, and cost per payload volume are the chosen metrics. The suitability of all technologies is briefly discussed regarding the case study mission. Ultimately, PCBSat is the most cost effective solution, as it is able to meet all mission requirements at a total mission cost of $264,590, which includes a ground station.

9.2 Assessment of Aims and Objectives

The two aims presented in Chapter 1 are used to guide the overall direction of this research. The first aim is *to advance the concept of space sensor networks*. The work presented in Chapter 3 achieves this aim, by suggesting a specific and relevant mission where this concept could be demonstrated, leading the way for future work. The second aim, *to determine the smallest practical cost-effective satellite in this context*, is clearly laid out in the remaining chapters. Although SpaceChip does not meet the minimum requirements of the case study, important contributions to system-on-a-chip technology have made a wider impact than originally envisaged, partially fulfilling this aim. PCBSat embodies the second aim completely, where the end result is the smallest satellite possible, using solely commercial resources to address every aspect of space systems engineering.

The specific objectives of this research, also presented in the introduction, now serve as the basis for assessing the success of the work. The first objective, *review and classify distributed space missions and systems*, is achieved in Chapter 2. Although many have discussed various aspects of this domain, a clarifying distributed space mission taxonomy is presented that equally highlights often overlooked massively distributed missions when compared to the excitement of formation flying concepts.

The second objective, *investigate existing and emerging very small satellite technologies*, is accomplished beginning in Chapter 2, where existing very small satellites are discussed,

specifically traditional picosatellites and microengineered aerospace systems. Two technologies are revived from previous investigations. Satellite-on-a-chip has been discussed in its earliest form since 1993, however little has been done at developing a complete system architecture, noting that data handling has seen some significant advancement. Chapter 4 goes on to present the first satellite-on-a-chip feasibility study at the system level, followed by the development of two essential subsystems in Chapter 5. Similarly, Chapter 6 revives an architecture similar to that used in Stensat of the 2000 OPAL picosatellite mission. Numerous advances in miniaturized commercial components now enable a capability not previously envisaged at this scale.

The third and fourth objectives, *propose a meaningful space sensor network mission as a case study* and *determine the critical mission requirements and architecture for the case study mission*, are completely developed in Chapter 3. The SMAD process is followed to investigate every aspect of a preliminary demonstration mission.

The fifth and sixth objectives, *develop supporting satellite technologies and system concepts* and *validate the work by designing, building, and characterising very small satellite prototypes*, are partially accomplished in Chapters 5 and completely in Chapter 6. These two chapters begin with the detailed mission requirements determined in Chapter 3 and attempt to develop very small satellite prototypes. The scale of effort required for a complete satellite-on-a-chip is beyond the capacity of an individual contribution, therefore a spectrum of issues was identified in Chapter 4 and two selected for further development in Chapter 5, supporting the SpaceChip concept. Chapters 6 and 7 are devoted to the design, build, and characterisation of PCBSat.

The final objective, *compare existing and newly developed technologies in this research for mission suitability, cost effectiveness, and mass producibility*, is attempted in Chapter 8. A first order cost model is presented, but is only intended to show order of magnitude, as many standard cost modelling practices are not feasible, such as capturing non-recurring engineering and time-accurate pricing adjustments.

9.3 Contributions to the State of the Art

Six novel contributions to the state of the art have been accomplished in this research by:

Identifying a range of sensor network missions that are enabled by very small satellites. A compilation of missions presented in Section 2.2.2.4 makes a compelling argument that numerous meaningful missions are awaiting space sensor network technologies to emerge.

Conducting the first feasibility study of the satellite-on-a-chip concept. Satellite-on-a-chip has remained the ultimate destination of satellite miniaturisation since 1993 and probably before. Furthermore, the term itself has been diluted from the pure literal form, eventually encompassing

a range of system integration technologies. This research presents a first-ever system-level feasibility assessment based on a monolithic system-on-a-chip approach, where complete SpaceChip satellites would literally roll off the automated semiconductor foundry process line in flyable form. The results of this research reveal that this approach falls short of meeting some of the most basic space mission requirements, due to its limited power generation, storage, and communication range, in addition to the lack of GPS and propulsion. However, numerous applications, such as wireless sensor networks and RFID, are beckoning for application in hostile environments, which includes space.

Developing a usable on-chip photovoltaic power supply for any system-on-a-chip. During the course of developing SpaceChip, a range of opportunities to develop supporting technologies emerged. One of the most acute shortfalls currently besetting progress is the lack of monolithically integrated photovoltaic or solar cells on commercial CMOS. After determining the obvious reason for this deficiency, which is not clearly reported on in the literature, a novel technique of using the common add-on bipolar junction transistor structure available in the SiGe BiCMOS process is developed. This approach allows not only the parallel connection of cells, but also series connections, which is not possible in bulk CMOS. Charge pumps or off-chip solutions are not needed. Three prototype chip efforts achieved a maximum efficiency of 3.44%; however, this approach requires more investigation before it can be applied to self-powering applications. Finally, this development supports a large range of applications; including Smart Dust scale wireless sensor networks, self-powered RFID, retinal implants, wildlife tagging and tracking, and many other applications requiring a self-powered system-on-a-chip implementation.

Verifying an environmentally tolerant design methodology for system-on-a-chip applications by combining radiation hardening by design and asynchronous logic. Although the general approach has been previously presented in the literature by the author and one other, the synergistic combination of these technologies had not yet been verified with quantitative results in hardware. Given an environment where radiation hardening by design must be used, accepting its power and area penalties, leveraging asynchronous logic reduces the power penalty by at least 45%. Additional techniques were implemented to flatten the power spectrum.

Designing, building, characterising, and testing a prototype very small satellite. Four prototyping efforts have evolved into a final configuration of 10×10×2.5 cm, 311 grams. Eight FR4 PCBs, two 6082-T6 aluminium plates, and two Delrin spacers are the primary structural materials, which serve to provide the P-POD compatible launch vehicle interface and protect the interior components from total radiation dose and thermal extremes. The MESA payload sensor plates are mounted on two adjacent sides, whose corner generally points in the velocity vector due to placing the centre of gravity in front of the centre of pressure, which is enhanced by deployable antennas conveniently placed. The EPS provides sufficient power to charge the batteries and

enable the radio during the sunlit portion of the orbit, so that MESA and GPS can operate during the eclipse. The DH subsystem collects payload and telemetry data at all phases of the mission, which is forwarded on command through the ad-hoc mesh network to the co-orbiting relay satellite.

Comparing all very small satellite technologies for mission suitability and cost-effectiveness. A first order cost model of very small satellites is developed and graphically illustrated. Depending on mission and payload requirements, better insight is available to the decision maker regarding the most cost-effective technology.

9.4 Future Work

Based on the efforts initiated in this research program, the following areas are proposed as logical extensions for further development of this technology area:

- Pursue demonstration mission opportunities offered by NASA on the Space Shuttle and ISS. Furthermore, the U.S. National Science Foundation has initiated a very small satellite based space weather research program [37] with multiple funding and flight opportunities. Launch opportunities are also emerging sponsored by ESA on the new Vega 1 launch vehicle.
- PCBSat is also well suited for educational environments, as the design allows for students to easily handle and interact with a real satellite at a low financial risk. Unlike EyasSat [253], which is targeted for undergraduate and graduate programs, PCBSat is well suited for secondary or perhaps primary education. The CMOS imager can be used as the primary payload along with the reduced-power XBee radio. PCBSat can be fitted with hobby-grade solar cells to reduce the cost to around $500, making it an affordable education tool.
- A practical approach to pursuing the completion and demonstration of the SpaceChip concept is required. More work is required on the system-level design, possibly investigating ADCS and thermal issues.
- Monolithic integrated radio transceiver research is a very exciting research area at the moment [123], however most SoC radios still require external passive devices, precision frequency oscillators, and antennas. Research is needed to determine if a very simple transceiver, perhaps using OOK modulation, could be implemented on CMOS without any external components [254]. However, it has been clearly demonstrated that an external antenna will be required to achieve any meaningful range.
- Emerging spacecraft-on-a-chip work at Cornell University is looking at a unique solution to propellantless manoeuvring by leveraging solar radiation pressure and Lorentz forces [255][256]. A collaboration should be established for mutual benefit.

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Appendix A. SpaceChip Simulation and Hardware Test Data

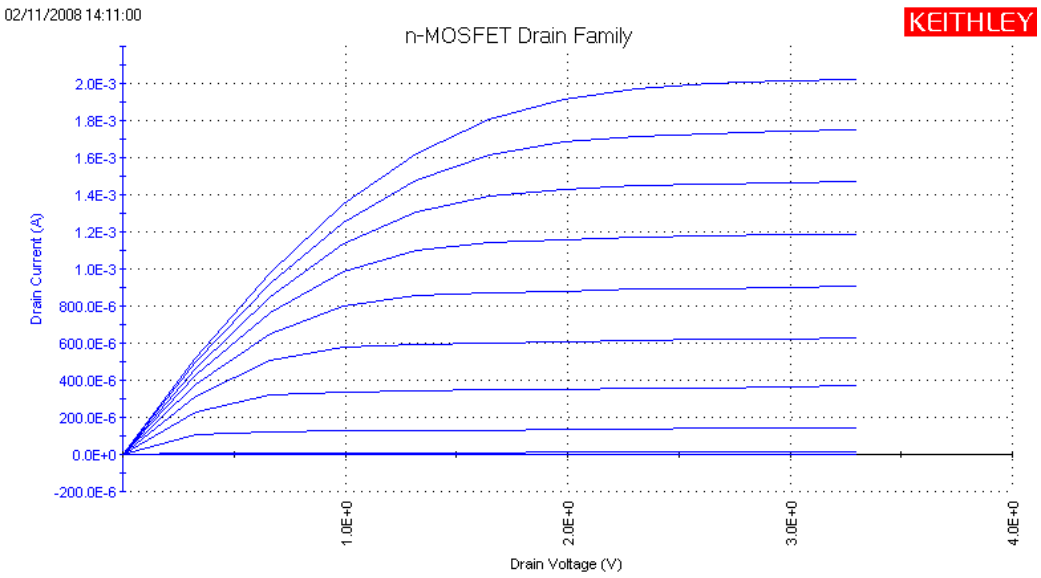


Figure A-1. Test Chip #2SC nMOS Drain Current vs. Drain to Source Voltage

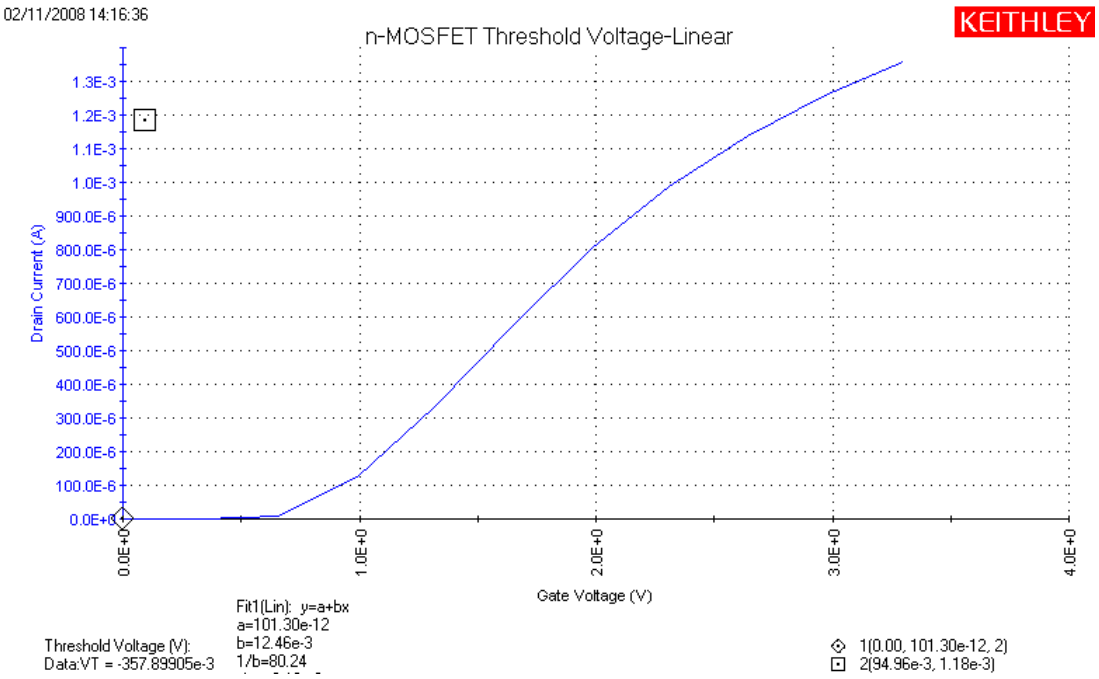


Figure A-2. Test Chip #2SC nMOS Linear Voltage Threshold

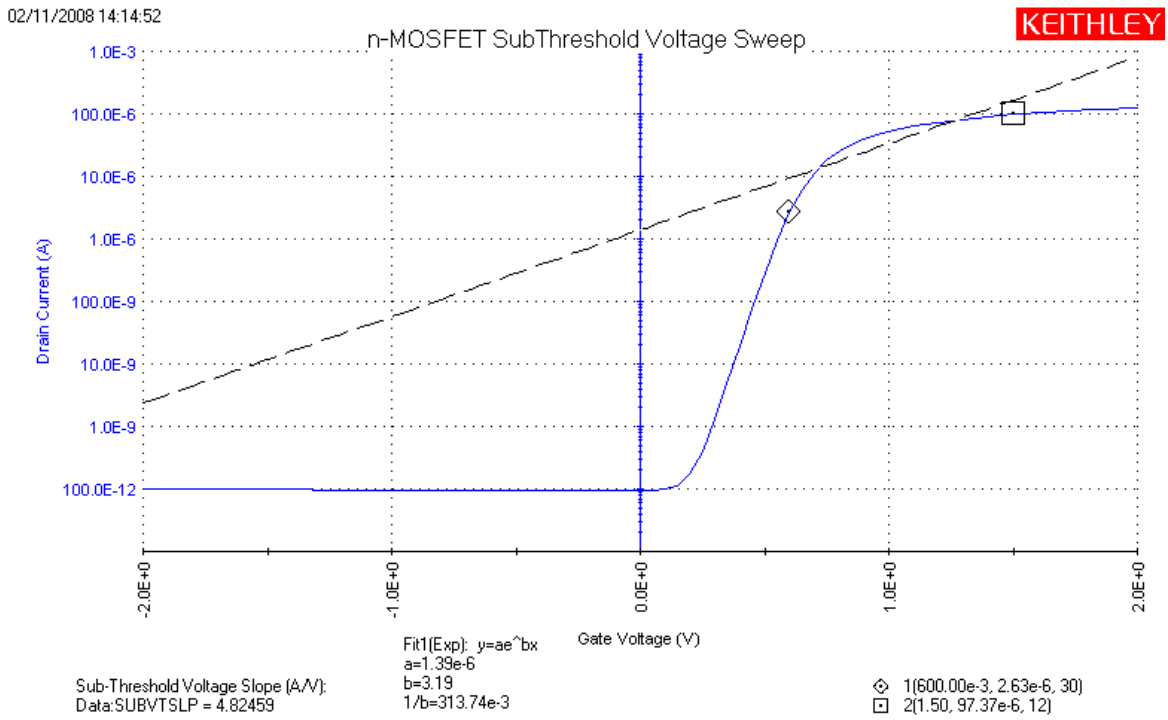


Figure A-3. Test Chip #2SC nMOS Subthreshold Voltage Threshold

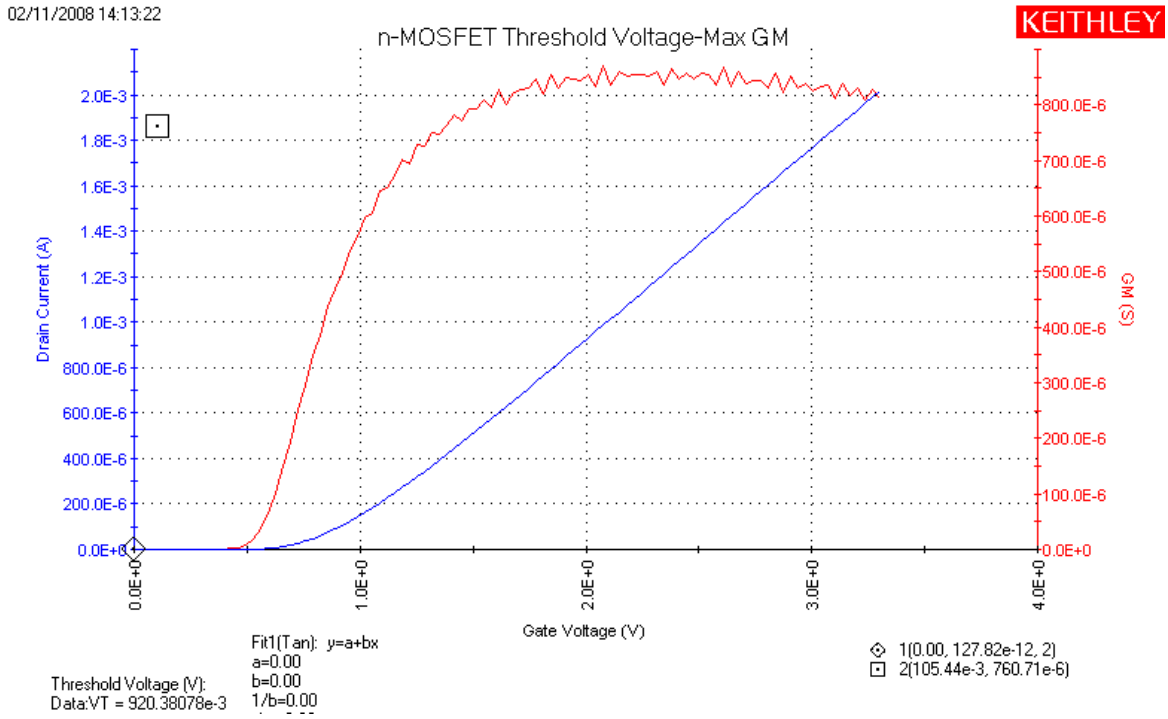


Figure A-4. Test Chip #2SC nMOS Drain Current vs. Gate to Source Voltage

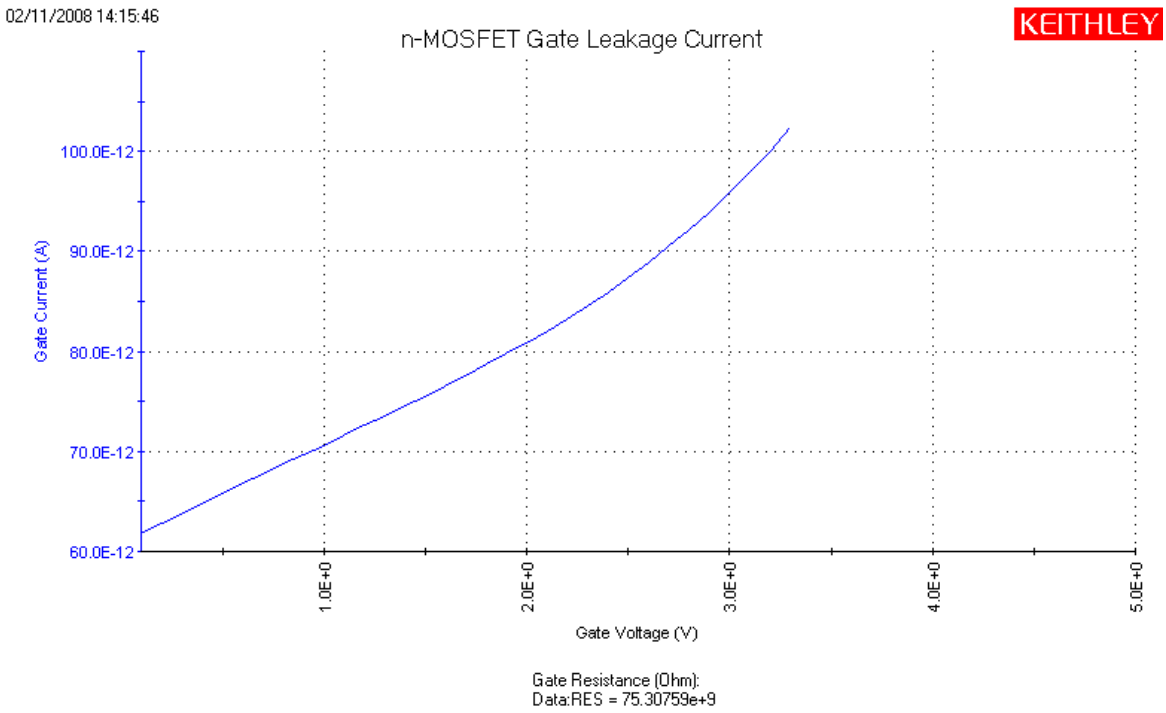


Figure A-5. Test Chip #2SC nMOS Gate Current vs. Gate Voltage

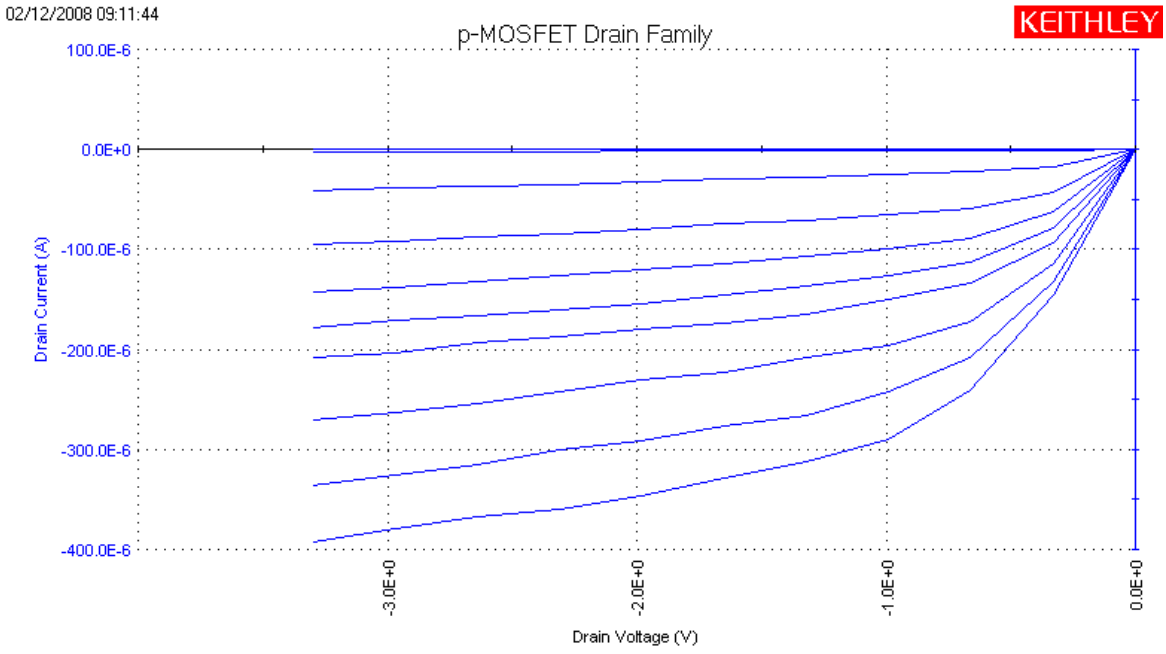


Figure A-6. Test Chip #2SC pMOS Drain Current vs. Drain to Source Voltage

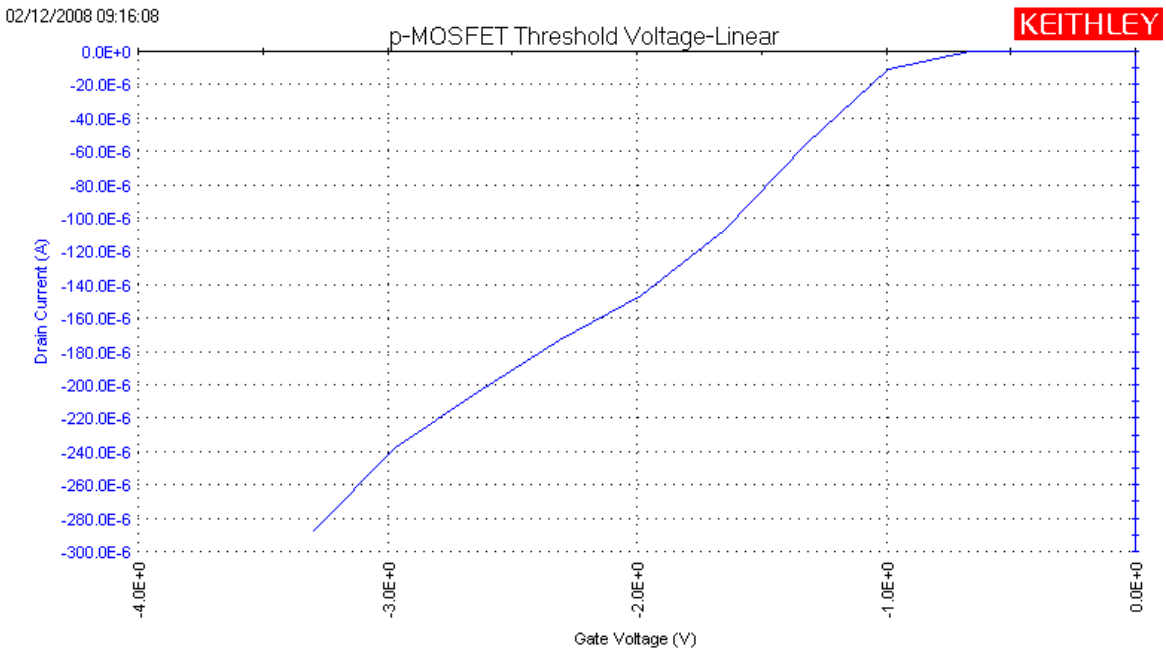


Figure A-7. Test Chip #2SC pMOS Linear Voltage Threshold

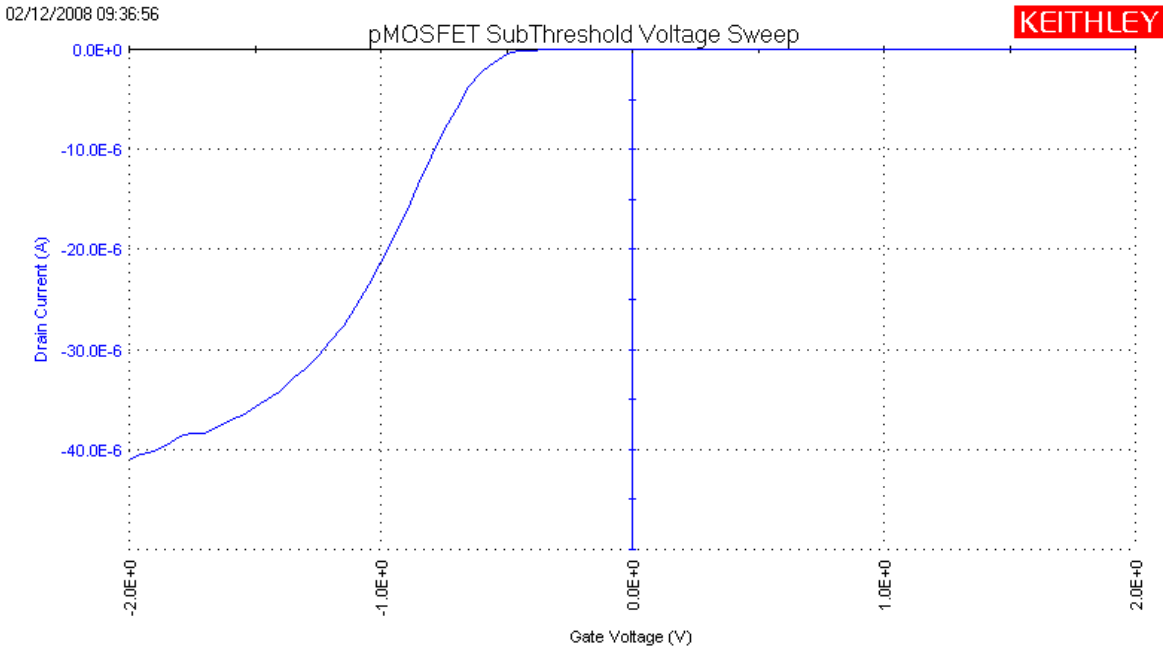


Figure A-8. Test Chip #2SC pMOS Subthreshold Voltage Threshold

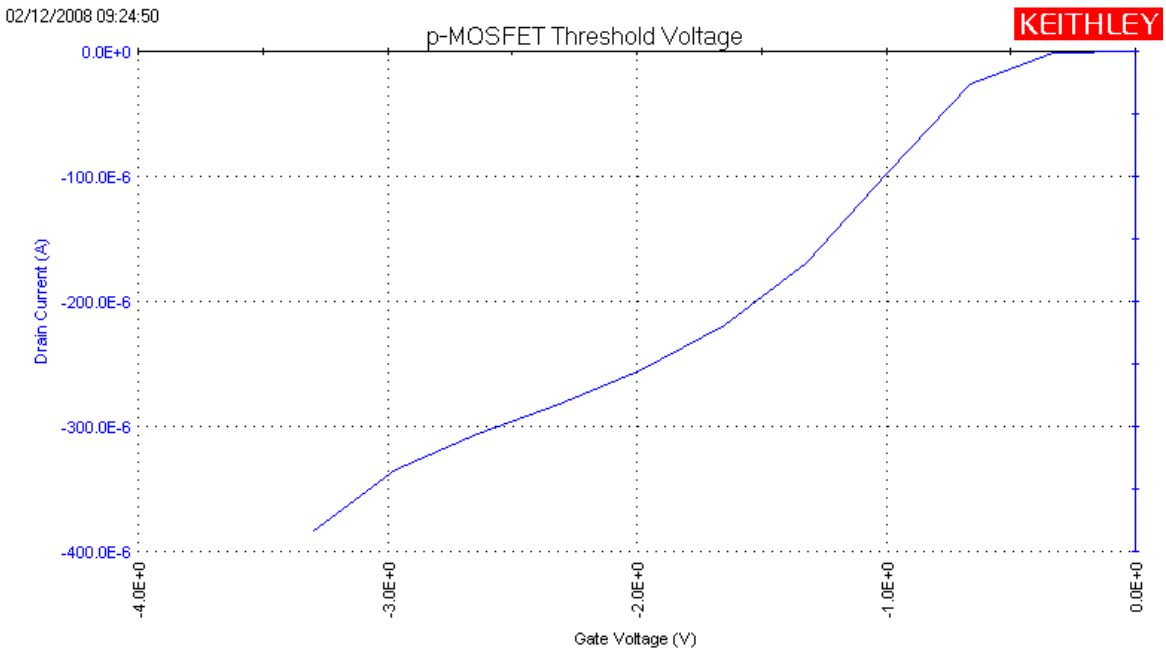


Figure A-9. Test Chip #2SC pMOS Drain Current vs. Gate to Source Voltage

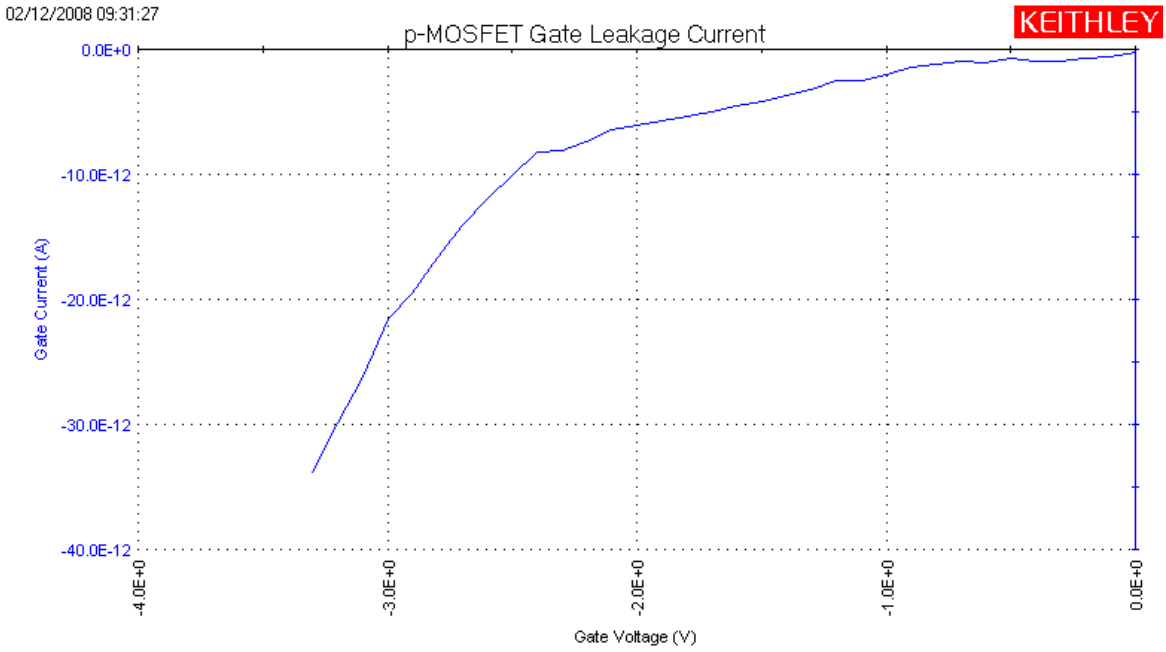


Figure A-10. Test Chip #2SC pMOS Gate Current vs. Gate Voltage

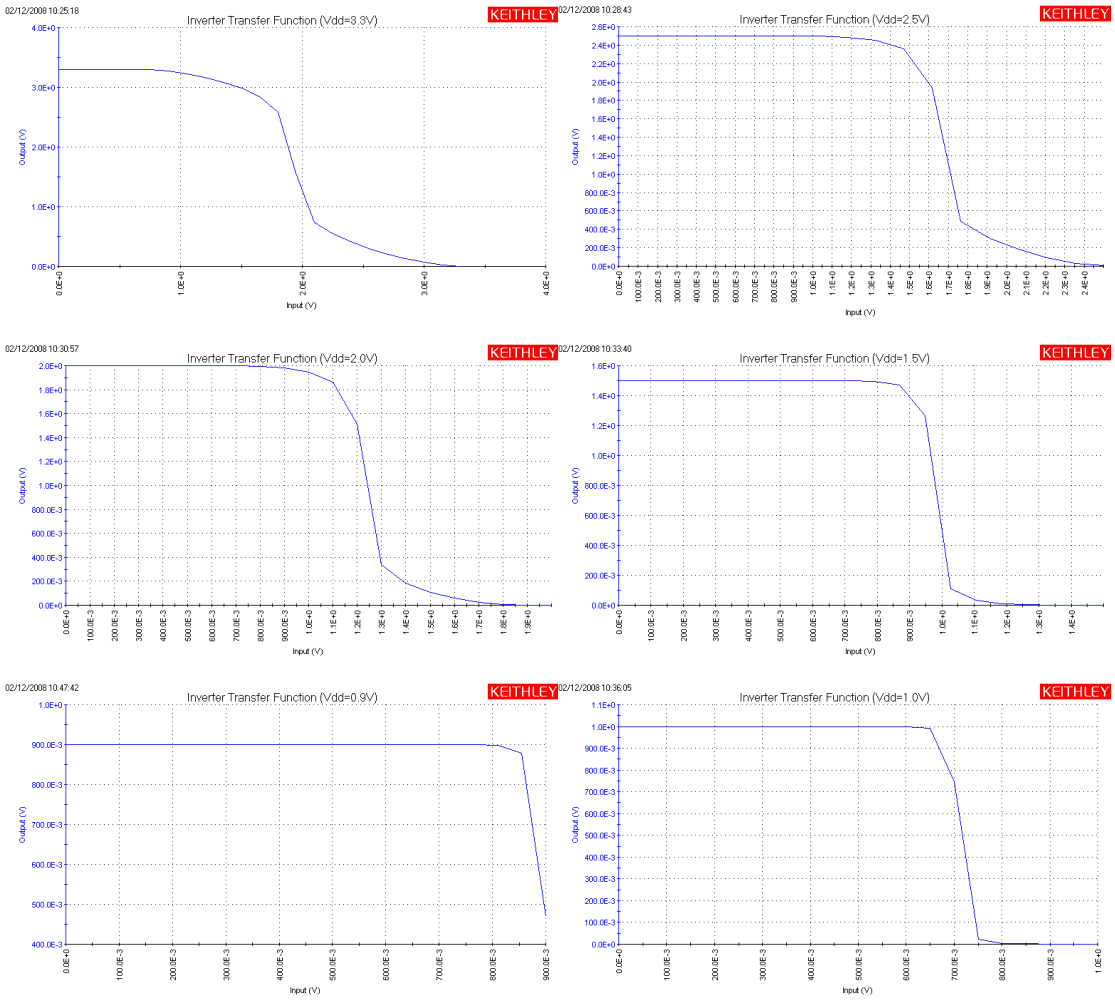


Figure A-11. Test Chip #2SC Minimum Inverter Operation Voltage

Table A-1. Test Chip Pinouts

Pin	SpaceChip1	SpaceChip2SC	SpaceChip2SR	SpaceChip2AR	SpaceChip3
1	PW3C	VDD (3.3V)	VDD (3.3V)	VDD (3.3V)	GND
2	PW2C	CLK	CLK	REQIN	NC
3	PW1C	RESET	RESET	RESET	NC
4	nMOS GND	PAD_TEST	PAD_TEST	PAD_TEST	TP2
5	nMOS S	BIDIR	BIDIR	BIDIR	TP4
6	nMOS D	DATA_ADDR0	DATA_ADDR0	DATA_ADDR0	TP6
7	nMOS G	DATA_ADDR1	DATA_ADDR1	DATA_ADDR1	NC
8	Inverter A	DATA_ADDR2	DATA_ADDR2	DATA_ADDR2	TP8
9	Inverter Q	DATA_ADDR3	DATA_ADDR3	DATA_ADDR3	NC
10	PW1E	DATA_ADDR4	DATA_ADDR4	DATA_ADDR4	NC
11	PW2E	DATA_ADDR5	DATA_ADDR5	DATA_ADDR5	TP9
12	PW3E	GND	GND	GND	TP7
13	BN1E	DATA_ADDR6	DATA_ADDR6	DATA_ADDR6	TP5
14	BN2E	DATA_ADDR7	DATA_ADDR7	DATA_ADDR7	TP3
15	BN3E	DATA_ADDR8	DATA_ADDR8	DATA_ADDR8	NC
16	Inverter GND	DATA_ADDR9	DATA_ADDR9	DATA_ADDR9	TP1
17	Inverter VDD	DATA_ADDR10	DATA_ADDR10	DATA_ADDR10	
18	pMOS G	DATA_ADDR11	DATA_ADDR11	DATA_ADDR11	
19	pMOS D	DATA_ADDR12	DATA_ADDR12	DATA_ADDR12	
20	pMOS S	DATA_ADDR13	DATA_ADDR13	DATA_ADDR13	
21	pMOS VDD	DATA_ADDR14	DATA_ADDR14	DATA_ADDR14	
22	BN3C	DATA_ADDR15	DATA_ADDR15	DATA_ADDR15	
23	BN2C	Solar Cell B	NC	PAD_TEST2	
24	BN1C	GND	GND	GND	
25		DATA_OUT0	DATA_OUT0	DATA_OUT0	
26		DATA_OUT1	DATA_OUT1	DATA_OUT1	
27		DATA_OUT2	DATA_OUT2	DATA_OUT2	
28		DATA_OUT3	DATA_OUT3	DATA_OUT3	
29		DATA_OUT4	DATA_OUT4	DATA_OUT4	
30		DATA_OUT5	DATA_OUT5	DATA_OUT5	
31		DATA_OUT6	DATA_OUT6	DATA_OUT6	
32		DATA_OUT7	DATA_OUT7	DATA_OUT7	
33		DATA_OUT8	DATA_OUT8	DATA_OUT8	
34		DATA_OUT9	DATA_OUT9	DATA_OUT9	
35		DATA_OUT10	DATA_OUT10	DATA_OUT10	
36		Solar Cell E	NC	REQOUT	
37		VDD	VDD	VDD	
38		DATA_OUT11	DATA_OUT11	DATA_OUT11	
39		DATA_OUT12	DATA_OUT12	DATA_OUT12	
40		DATA_OUT13	DATA_OUT13	DATA_OUT13	
41		DATA_OUT14	DATA_OUT14	DATA_OUT14	
42		DATA_OUT15	DATA_OUT15	DATA_OUT15	
43		PSTATE3	PSTATE3	PSTATE3	
44		PSTATE2	PSTATE2	PSTATE2	
45		PSTATE1	PSTATE1	PSTATE1	
46		PSTATE0	PSTATE0	PSTATE0	
47		MEMWRITE	MEMWRITE	MEMWRITE	
48		MEMREAD	MEMREAD	MEMREAD	

Figure A-12. NC-Verilog Testbench

```
`timescale 1ns / 1ps

module test;

wire  MEMREAD, MEMWRITE, PAD_TEST, REQOUT;
reg  BIDIR, CLK, RESET;
wire [15:0]  DATA_OUT;
wire [3:0]  PSTATE;
wire [15:0]  DATA_ADDR;
reg  [15:0] io_DATA_ADDR;
cds_alias #(16) cds_alias_inst1(DATA_ADDR, io_DATA_ADDR);

//--------------------opcdrsrtrdstfunc
reg [15:0] zR   = 16'b0000000000000000;

//--------------------opcdrsrtaddresss
reg [15:0] zLW1 = 16'b0001000100000001; //load register 1 from address 1
reg [15:0] zLW2 = 16'b0001001000000010; //load register 2 from address 2
reg [15:0] zRTA = 16'b0000011011000000; //add reg 1 to reg 2 store reg 3
reg [15:0] zSW3 = 16'b0010001100000000; //store register 3 to address 0
reg [15:0] zRTS = 16'b0000011011000010; //sub reg 1 from reg 2 store reg
3
reg [15:0] zRTN = 16'b0000011011000100; //and reg 1 with reg 2 store reg
3
reg [15:0] zRTO = 16'b0000011011000101; //or  reg 1 with reg 2 store reg
3
reg [15:0] zRTT = 16'b0000011011001010; //slt reg 1 with reg 2 store reg
3
reg [15:0] zBEQ = 16'b0011011010101010; //beq reg 1 with reg 2 address
0;
reg [15:0] zJMP = 16'b0100000000000000; //jmp to address 0;

integer CP;

top top(DATA_OUT, MEMREAD, MEMWRITE, PAD_TEST, PSTATE, REQOUT,
     DATA_ADDR, BIDIR, CLK, RESET);

initial begin

CP = 60; //clock period in nanoseconds

 #0 RESET = 1; CLK = 0; io_DATA_ADDR = zLW1; BIDIR=1;
 #(CP/2+12) RESET = 0;
 #(CP*3-12) io_DATA_ADDR = 16'hFFFF;
 #(CP*2) io_DATA_ADDR = zLW2;
 #(CP*3) io_DATA_ADDR = 16'h0001;
 #(CP*2) io_DATA_ADDR = zRTA;
 #(CP*4) io_DATA_ADDR = zSW3;
 #(CP*4) io_DATA_ADDR = zRTS;
 #(CP*4) io_DATA_ADDR = zSW3;
 #(CP*4) io_DATA_ADDR = zRTN;
 #(CP*4) io_DATA_ADDR = zSW3;
 #(CP*4) io_DATA_ADDR = zRTO;
 #(CP*4) io_DATA_ADDR = zSW3;
 #(CP*4) io_DATA_ADDR = zRTT;
 #(CP*4) io_DATA_ADDR = zSW3;
 #(CP*4) io_DATA_ADDR = zBEQ;
 #(CP*3) io_DATA_ADDR = zLW2;
```

```
 #(CP*3) io_DATA_ADDR = 16'hFFFF;
 #(CP*2) io_DATA_ADDR = zRTT;
 #(CP*4) io_DATA_ADDR = zSW3;
 #(CP*4) io_DATA_ADDR = zBEQ;
 #(CP*3) io_DATA_ADDR = zJMP;
 #(CP*6) $finish;
end

//while (RESET == 0) begin
// wait (CLOCK)
//  io_DATA_ADDR = 16'hFFFF;
//end

always
 #(CP/2) CLK = !CLK;
endmodule
```

			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
frequency in MHz		1.25																	
clock period in nanoseconds		800																	
#0 RESET = 1; CLK = 1; BIDIR = 1; io_DATA_ADDR = zLW1;		0	0	0	0	1	0	0	0	1	0	0	0	0	0	0	0	1	1101
#(CP+1) RESET = 0;		801																	
#(CP*3-CP/2-1) io_DATA_ADDR = 16'hFFFF;		2800	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	ffff
#(CP*2) io_DATA_ADDR = zLW2;		4400	0	0	0	1	0	0	1	0	0	0	0	0	0	0	1	0	1202
#(CP*3) io_DATA_ADDR = 16'h0001;		6800	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0001
#(CP*2) io_DATA_ADDR = zRTA;		8400	0	0	0	0	0	1	1	0	1	1	0	0	0	0	0	0	06c0
#(CP*4) io_DATA_ADDR = zSW3;		11600	0	0	1	0	0	0	1	1	0	0	0	0	0	0	0	0	2300
#(CP*4) io_DATA_ADDR = zRTS;		14800	0	0	0	0	0	1	1	0	1	1	0	0	0	0	1	0	06c2
#(CP*4) io_DATA_ADDR = zSW3;		18000	0	0	1	0	0	0	1	1	0	0	0	0	0	0	0	0	2300
#(CP*4) io_DATA_ADDR = zRTN;		21200	0	0	0	0	0	1	1	0	1	1	0	0	0	1	0	0	06c4
#(CP*4) io_DATA_ADDR = zSW3;		24400	0	0	1	0	0	0	1	1	0	0	0	0	0	0	0	0	2300
#(CP*4) io_DATA_ADDR = zRTO;		27600	0	0	0	0	0	1	1	0	1	1	0	0	0	1	0	1	06c5
#(CP*4) io_DATA_ADDR = zSW3;		30800	0	0	1	0	0	0	1	1	0	0	0	0	0	0	0	0	2300
#(CP*4) io_DATA_ADDR = zRTT;		34000	0	0	0	0	0	1	1	0	1	1	0	0	1	0	1	0	06ca
#(CP*4) io_DATA_ADDR = zSW3;		37200	0	0	1	0	0	0	1	1	0	0	0	0	0	0	0	0	2300
#(CP*4) io_DATA_ADDR = zBEQ;		40400	0	0	1	1	0	1	1	0	1	0	1	0	1	0	1	0	36aa
#(CP*3) io_DATA_ADDR = zLW2;		42800	0	0	0	1	0	0	1	0	0	0	0	0	0	0	1	0	1202
#(CP*3) io_DATA_ADDR = 16'hFFFF;		45200	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	ffff
#(CP*2) io_DATA_ADDR = zRTT;		46800	0	0	0	0	0	1	1	0	1	1	0	0	1	0	1	0	06ca
#(CP*4) io_DATA_ADDR = zSW3;		50000	0	0	1	0	0	0	1	1	0	0	0	0	0	0	0	0	2300
#(CP*4) io_DATA_ADDR = zBEQ;		53200	0	0	1	1	0	1	1	0	1	0	1	0	1	0	1	0	36aa
#(CP*3) io_DATA_ADDR = zJMP;		55600	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	4000
#(CP*6) $finish;	UltraSim.sim	**60400**																	
end																			
always																			
#(CP/2) CLK = !CLK;																			
reg [15:0] zLW1 = 16'b0001000100000001; //load register 1 from address 1			0	0	0	1	0	0	0	1	0	0	0	0	0	0	0	1	
reg [15:0] zLW2 = 16'b0001001000000010; //load register 2 from address 2			0	0	0	1	0	0	1	0	0	0	0	0	0	0	1	0	
reg [15:0] zRTA = 16'b0000011011000000; //add reg 1 to reg 2 store reg 3			0	0	0	0	0	1	1	0	1	1	0	0	0	0	0	0	
reg [15:0] zSW3 = 16'b0010001100000000; //store register 3 to address 0			0	0	1	0	0	0	1	1	0	0	0	0	0	0	0	0	
reg [15:0] zRTS = 16'b0000011011000010; //sub reg 1 from reg 2 store reg 3			0	0	0	0	0	1	1	0	1	1	0	0	0	0	1	0	
reg [15:0] zRTN = 16'b0000011011000100; //and reg 1 with reg 2 store reg 3			0	0	0	0	0	1	1	0	1	1	0	0	0	1	0	0	
reg [15:0] zRTO = 16'b0000011011000101; //or reg 1 with reg 2 store reg 3			0	0	0	0	0	1	1	0	1	1	0	0	0	1	0	1	
reg [15:0] zRTT = 16'b0000011011001010; //slt reg 1 with reg 2 store reg 3			0	0	0	0	0	1	1	0	1	1	0	0	1	0	1	0	
reg [15:0] zBEQ = 16'b0011011010101010; //beq reg 1 with reg 2 address 0;			0	0	1	1	0	1	1	0	1	0	1	0	1	0	1	0	
reg [15:0] zJMP = 16'b0100000000000000; //jmp to address 0;			0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

Figure A-13. UltraSim Testbench

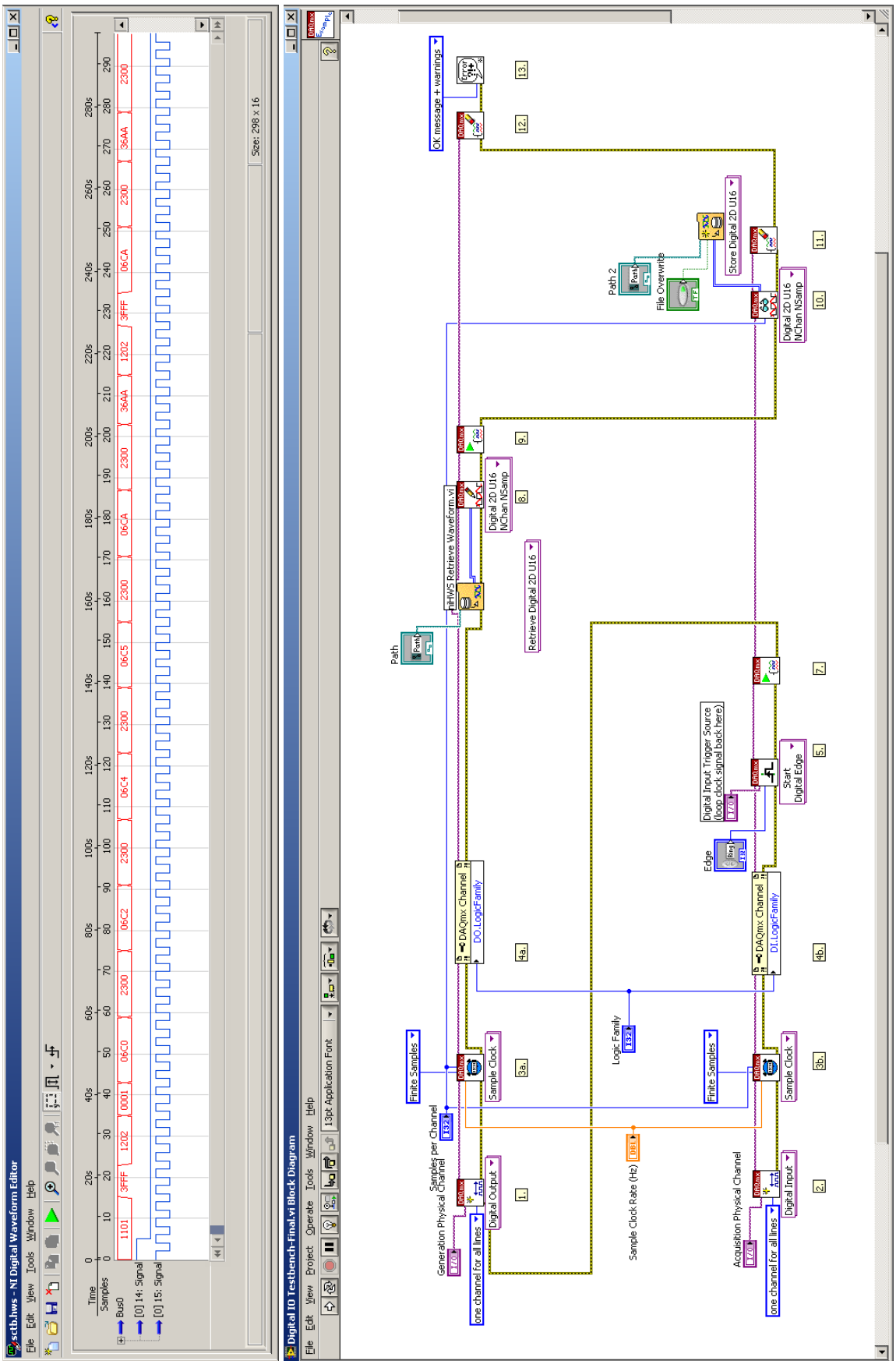


Figure A-14. Digital Waveform Editor Testbench and LabView Testbench Code

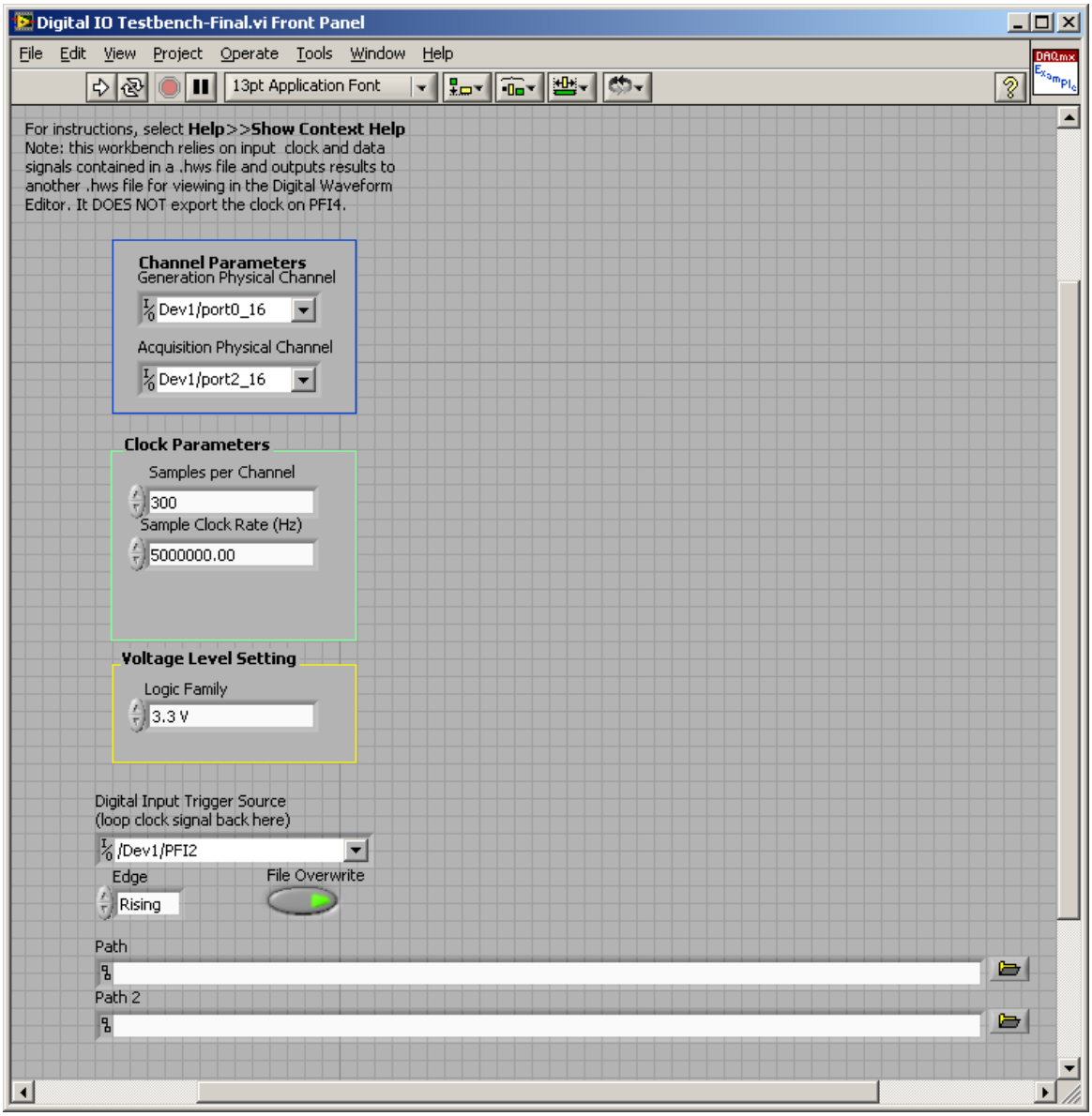


Figure A-15. Digital Waveform Editor Testbench Control Panel

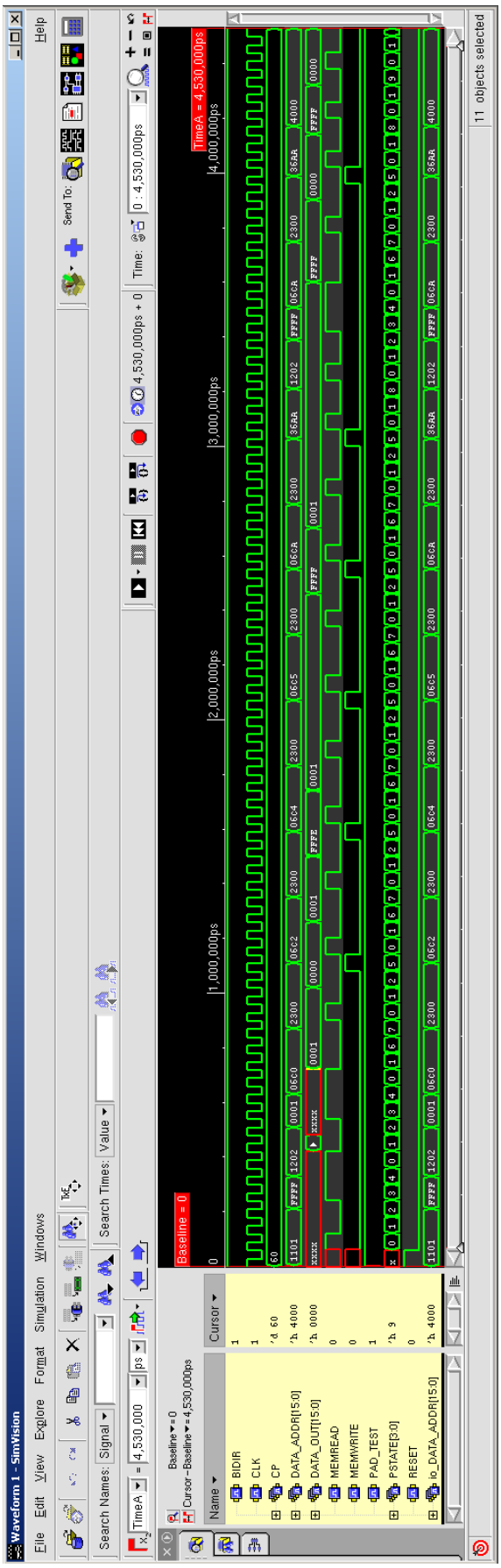


Figure A-16. Test Chip #2SC NC-Verilog Functional

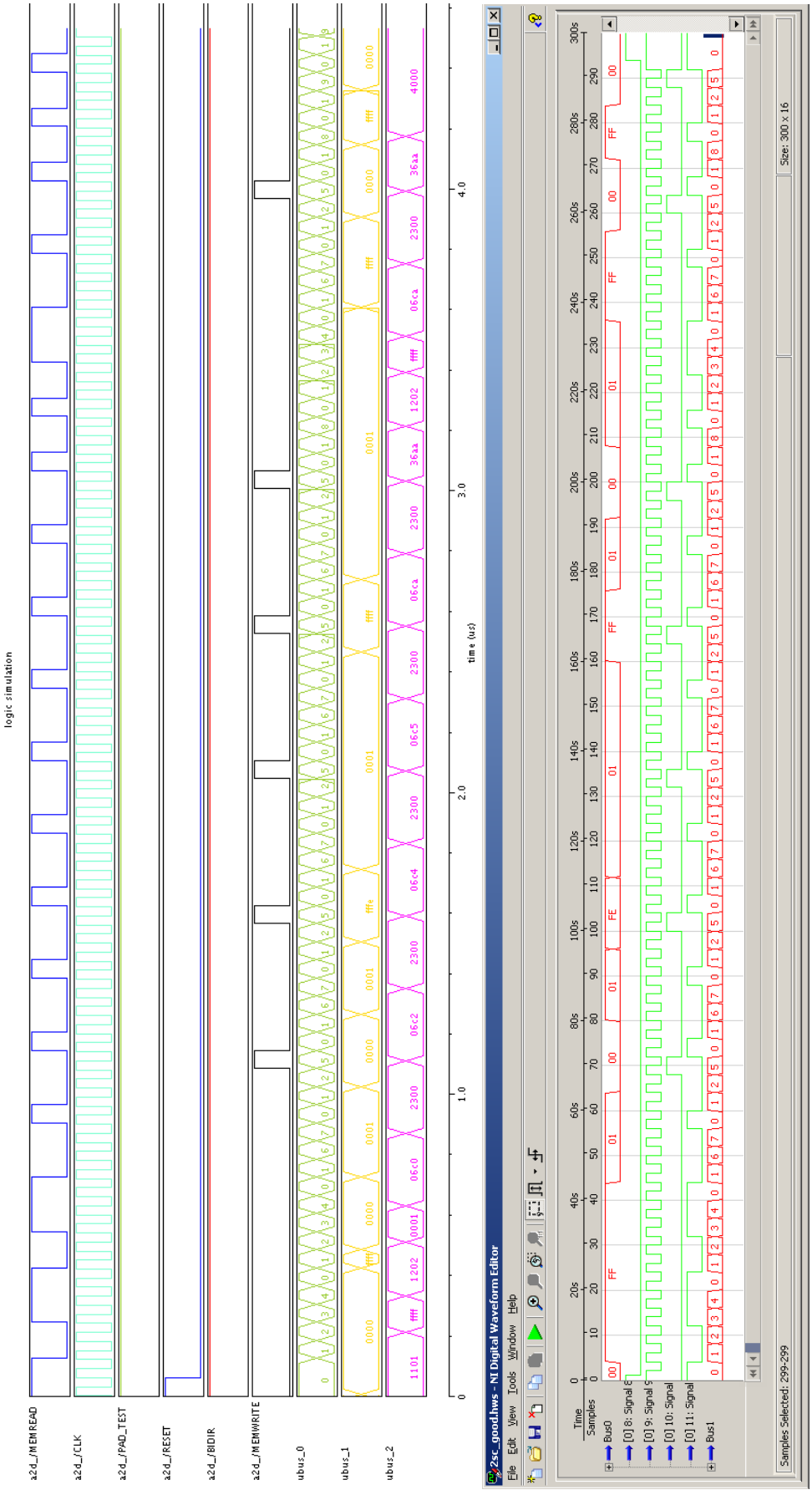


Figure A-17. Test Chip #2SC UltraSim (left) and Hardware (right) Functional

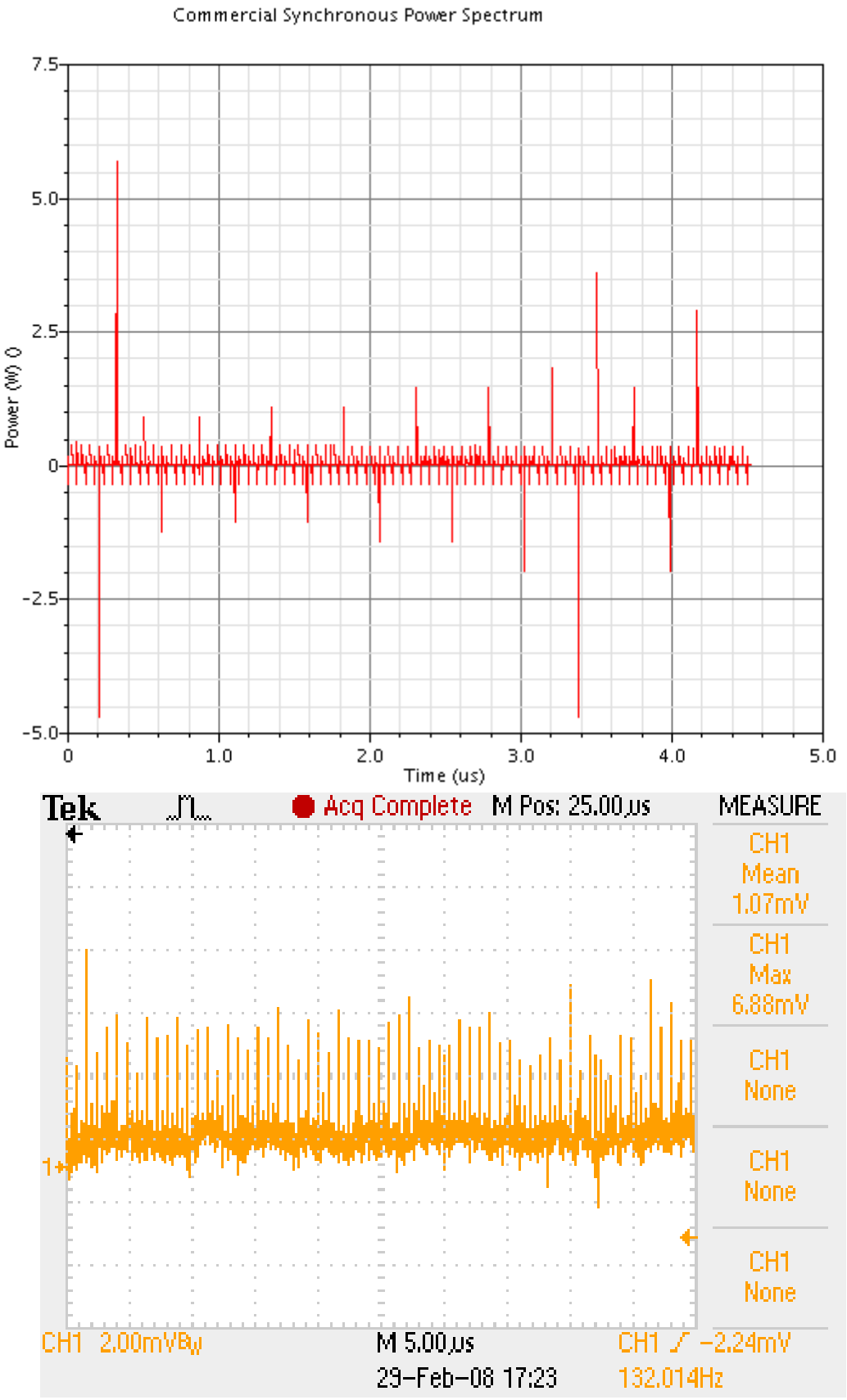


Figure A-18. Test Chip #2SC UltraSim/Hardware Power Comparison (full)

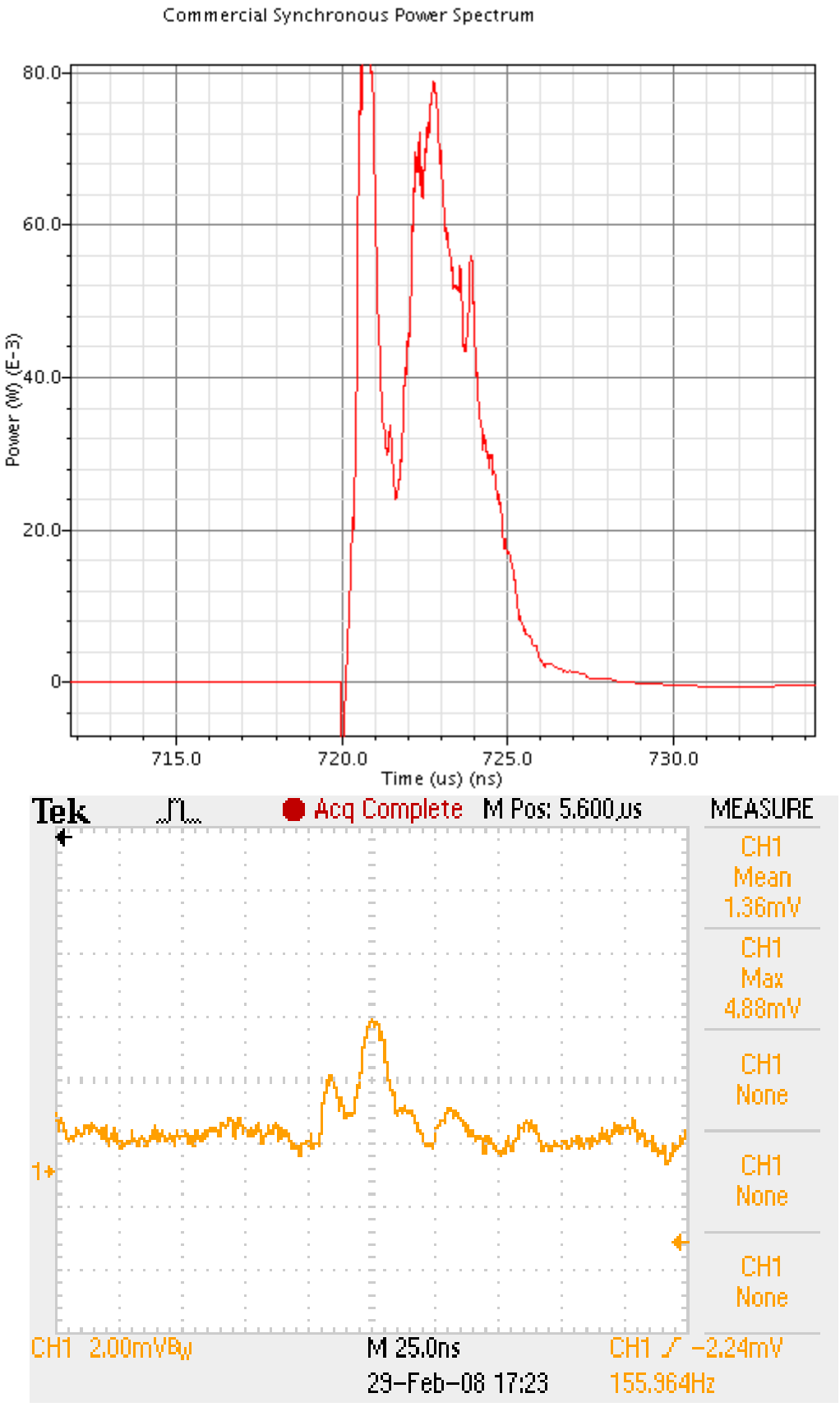


Figure A-19. Test Chip #2SC UltraSim/Hardware Power Comparison (single)

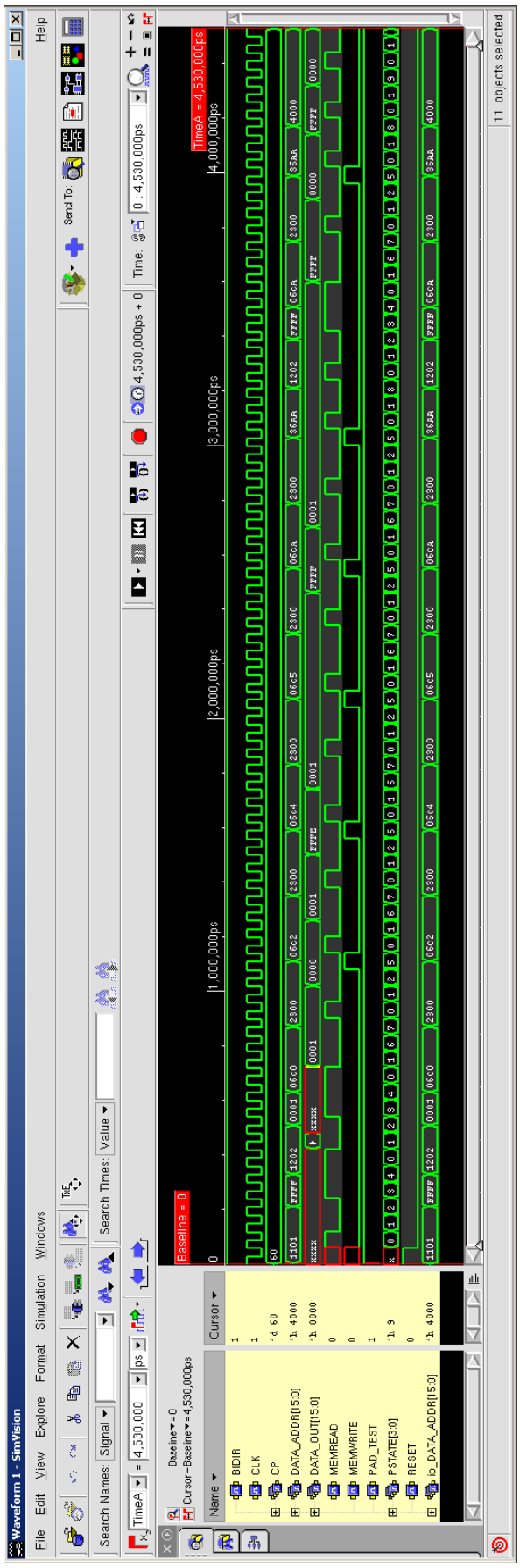


Figure A-20. Test Chip #2SR NC-Verilog Functional

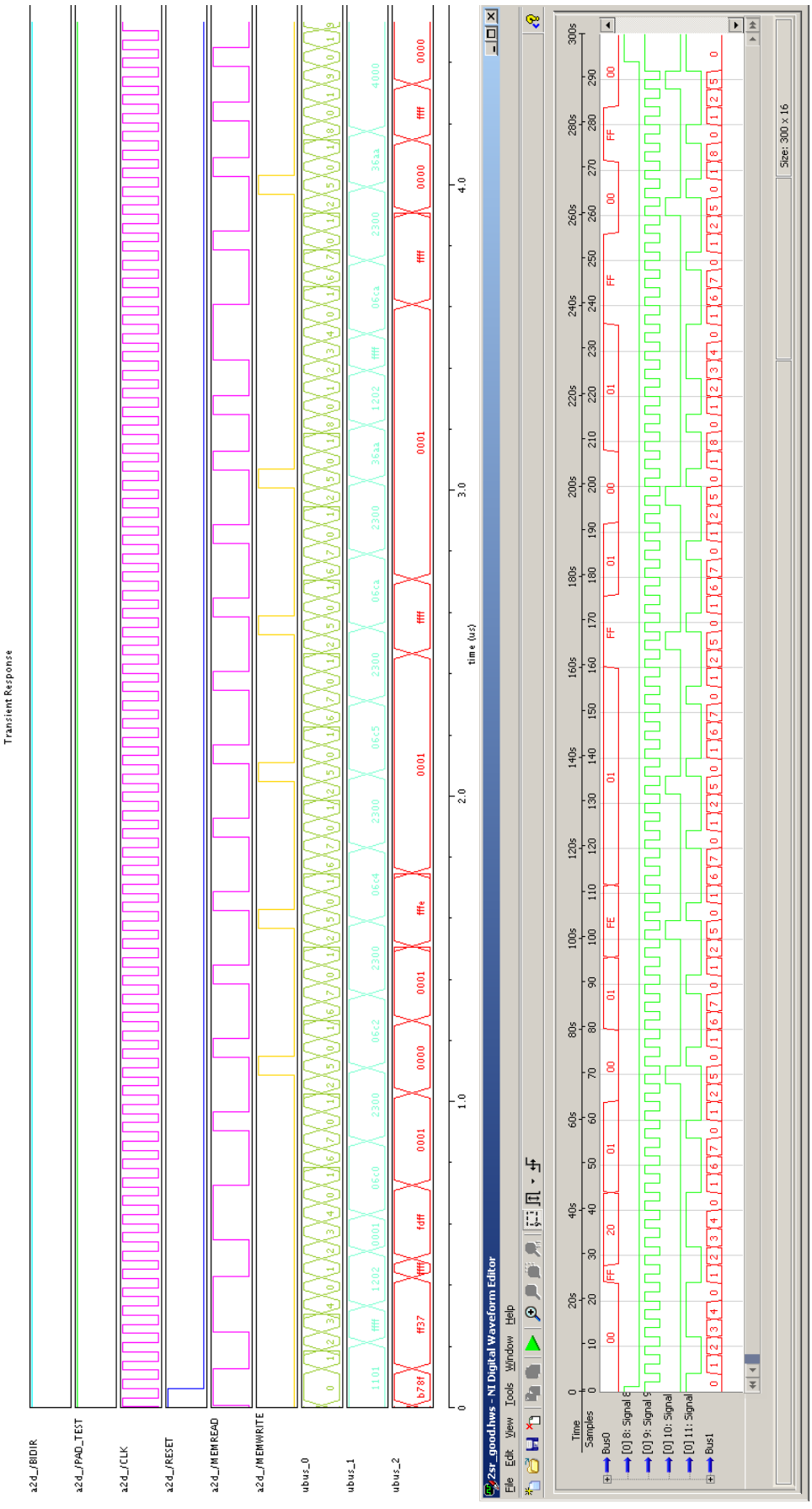


Figure A-21. Test Chip #2SR UltraSim (left) and Hardware (right) Functional

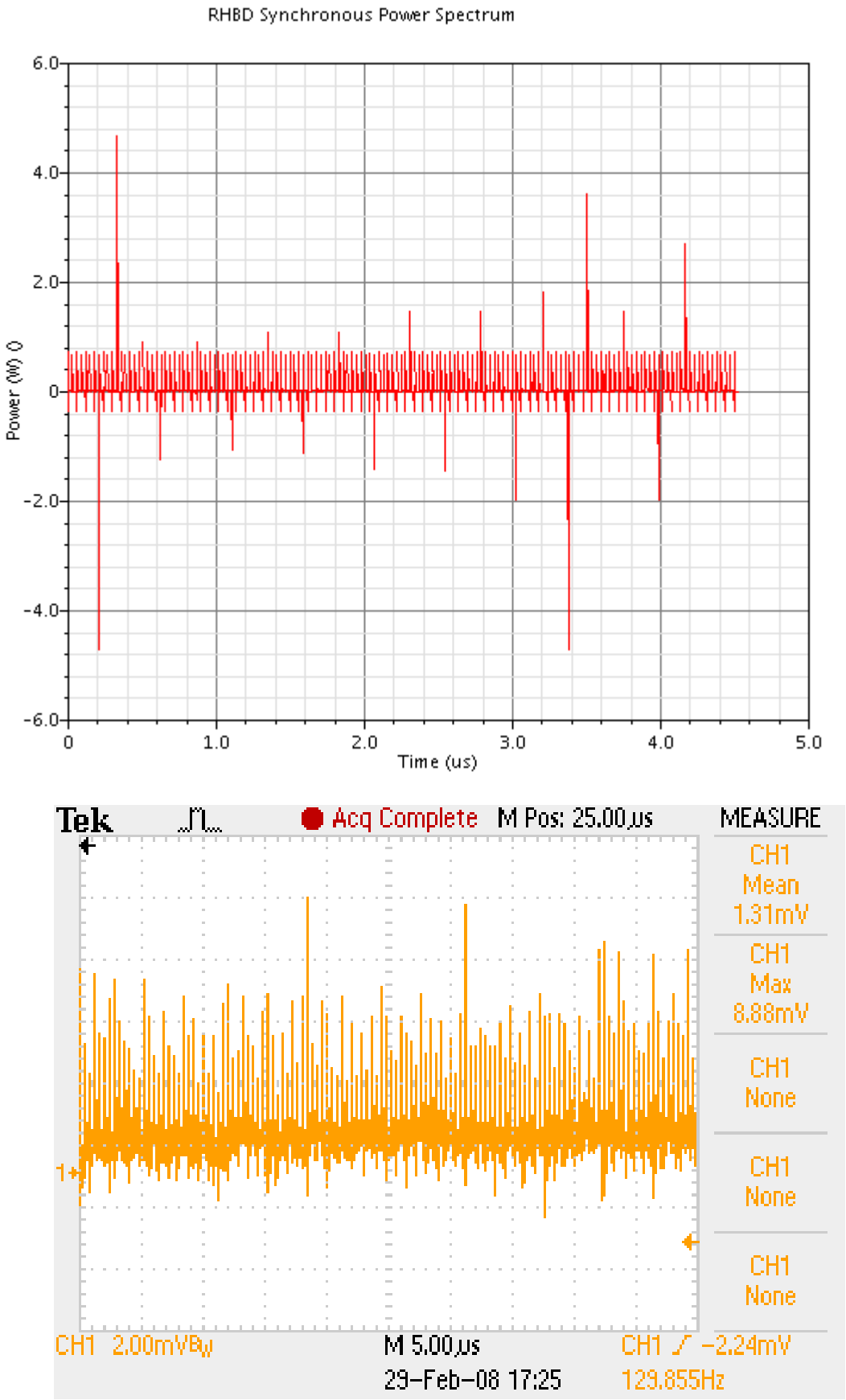


Figure A-22. Test Chip #2SR UltraSim/Hardware Power Comparison (full)

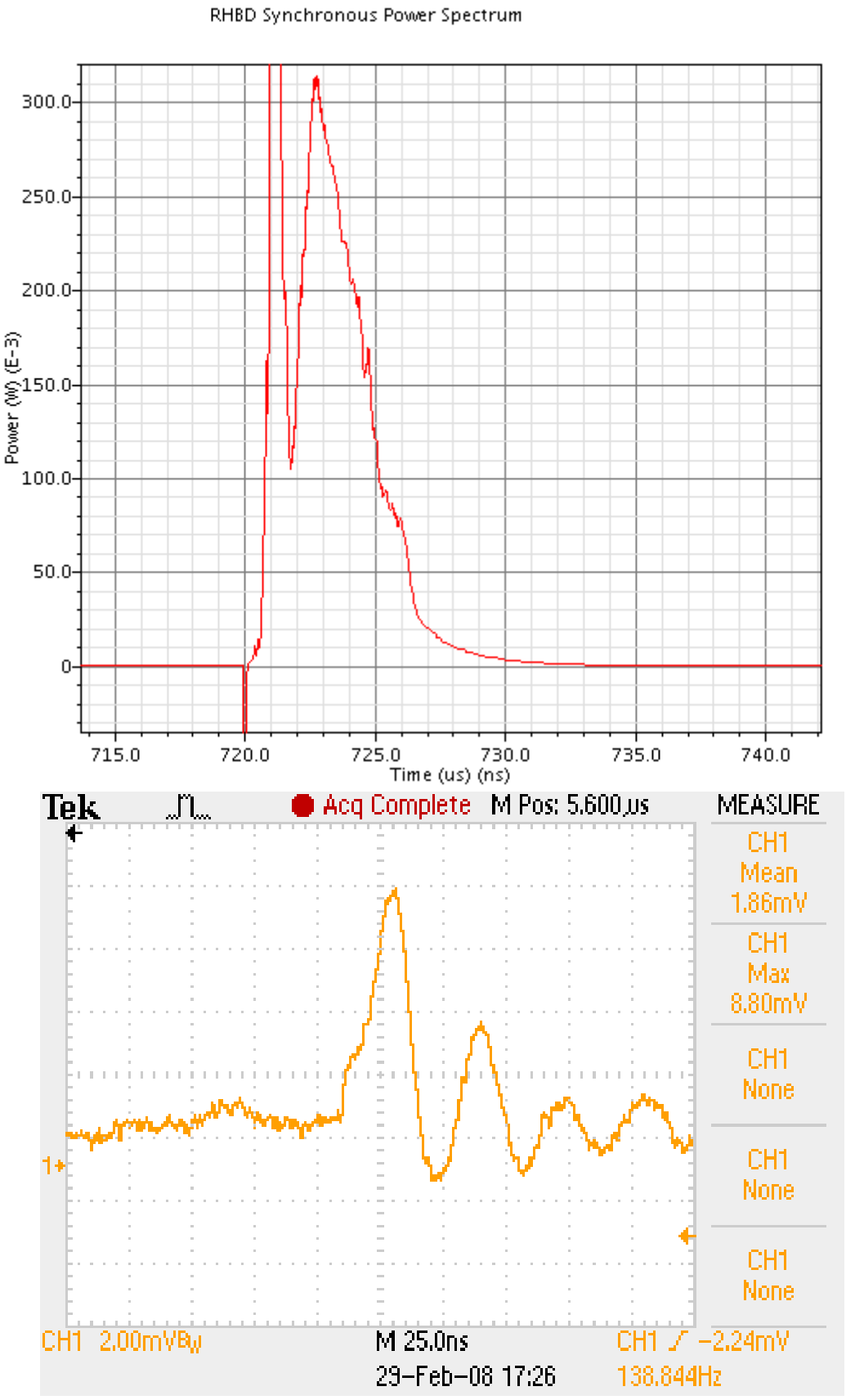


Figure A-23. Test Chip #2SR UltraSim/Hardware Power Comparison (single)

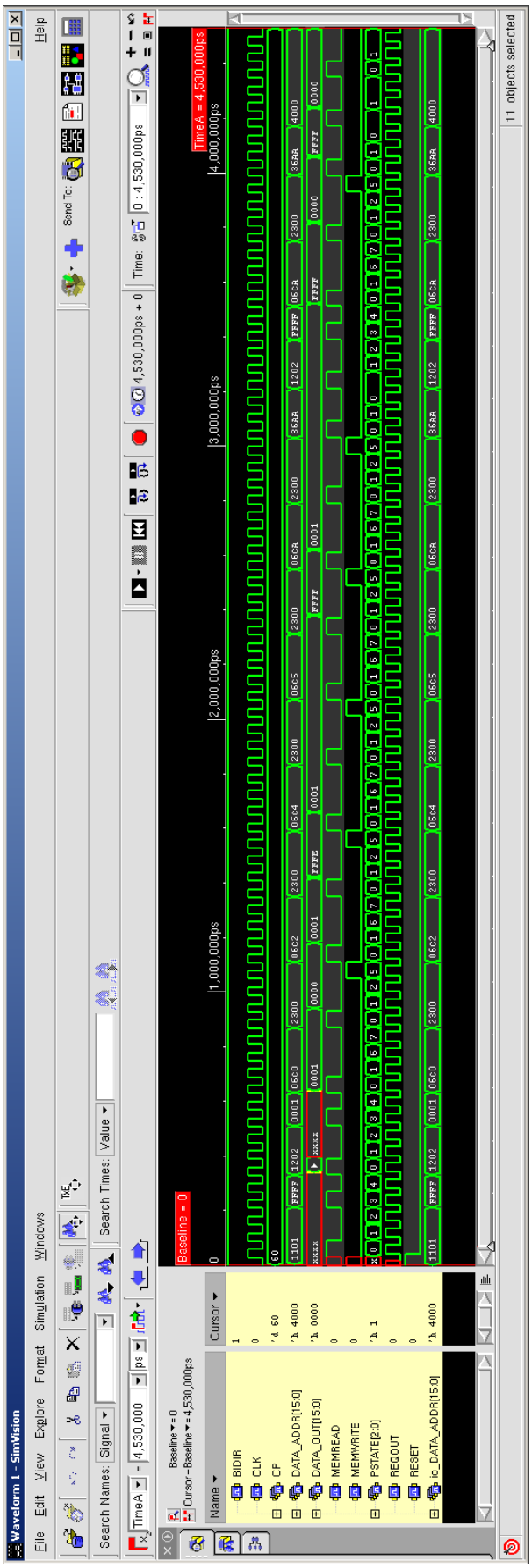


Figure A-24. Test Chip #2AR NC-Verilog Functional

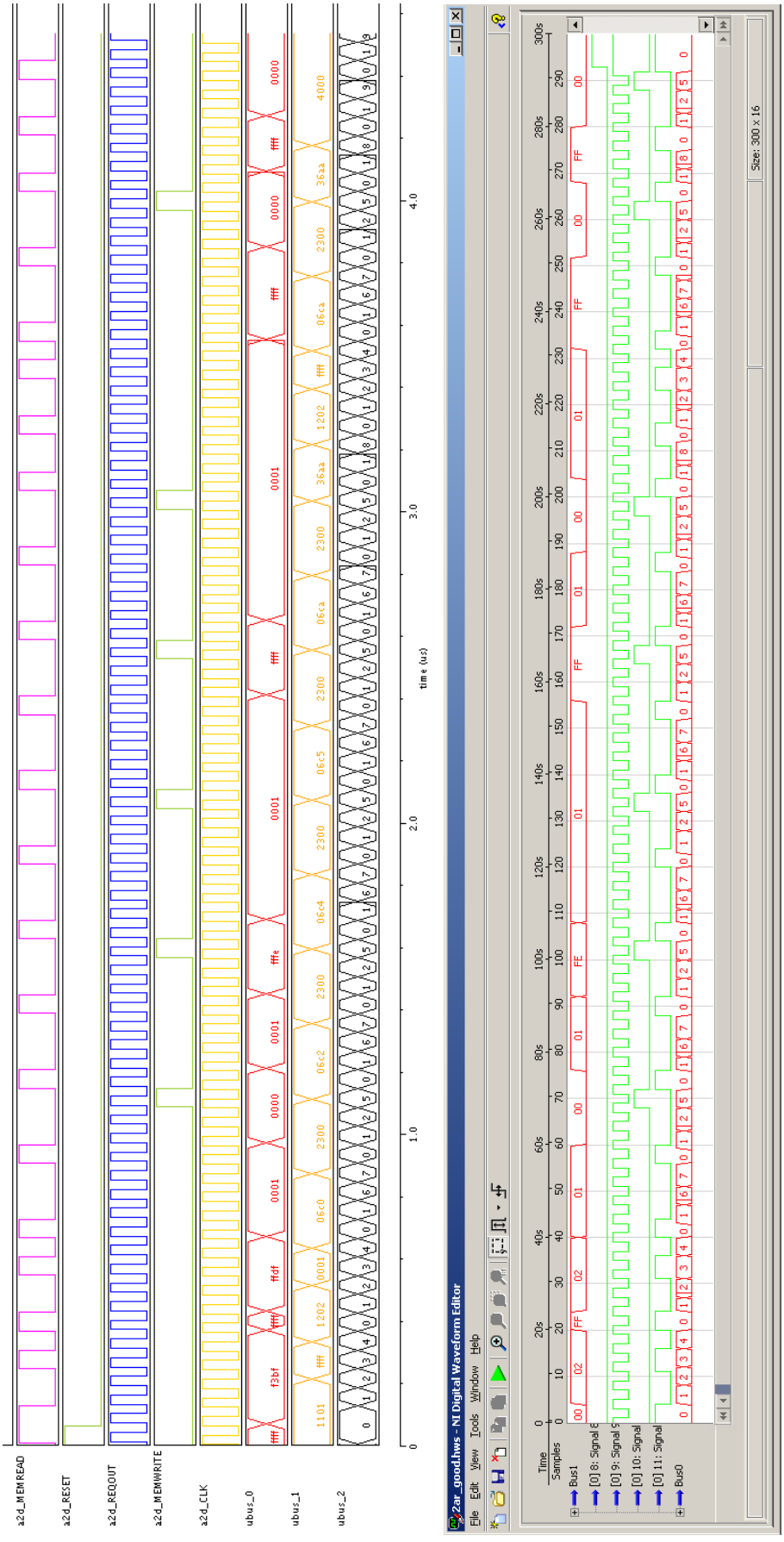


Figure A-25. Test Chip #2AR UltraSim (left) and Hardware (right) Functional

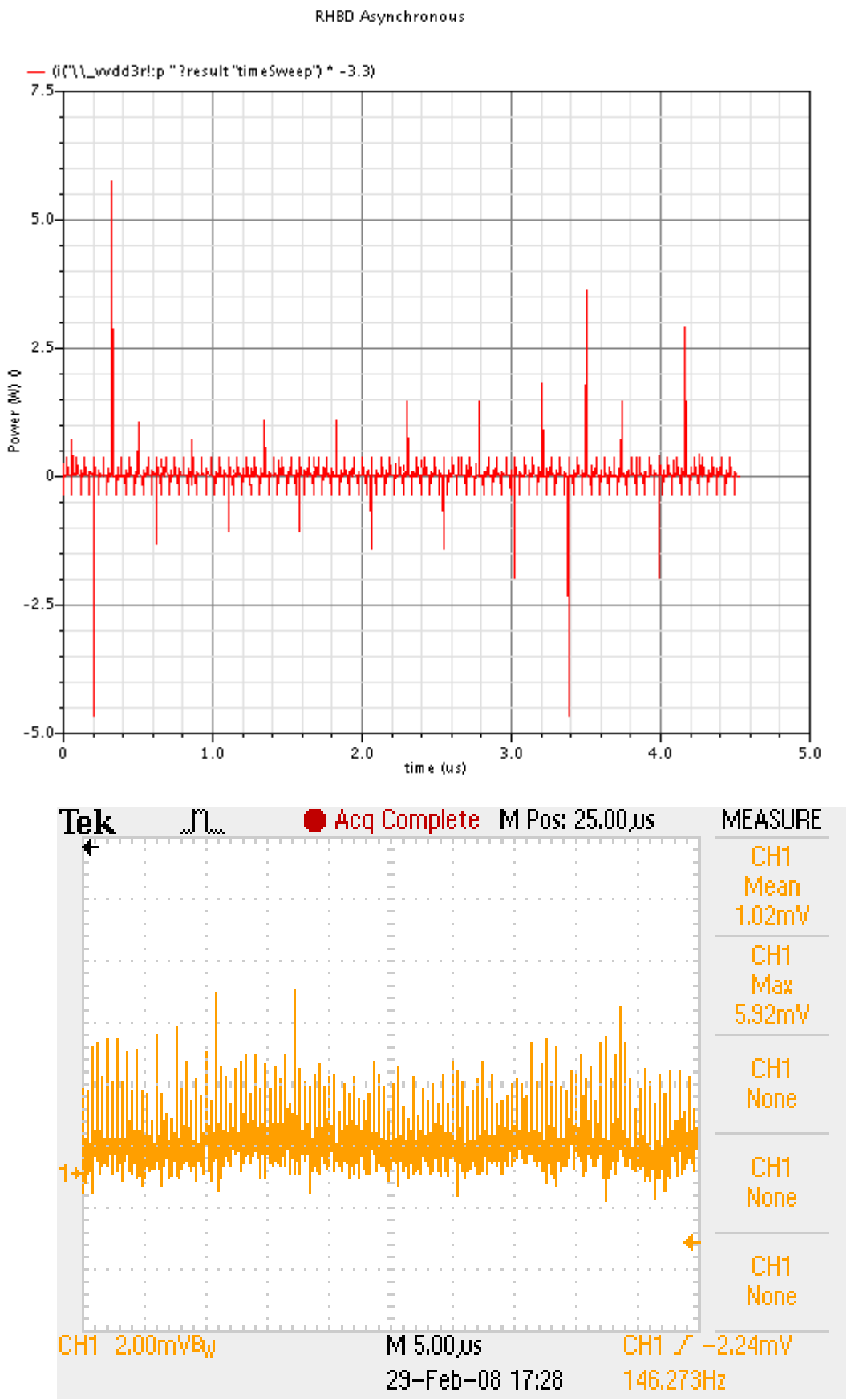


Figure A-26. Test Chip #2AR UltraSim/Hardware Power Comparison (full)

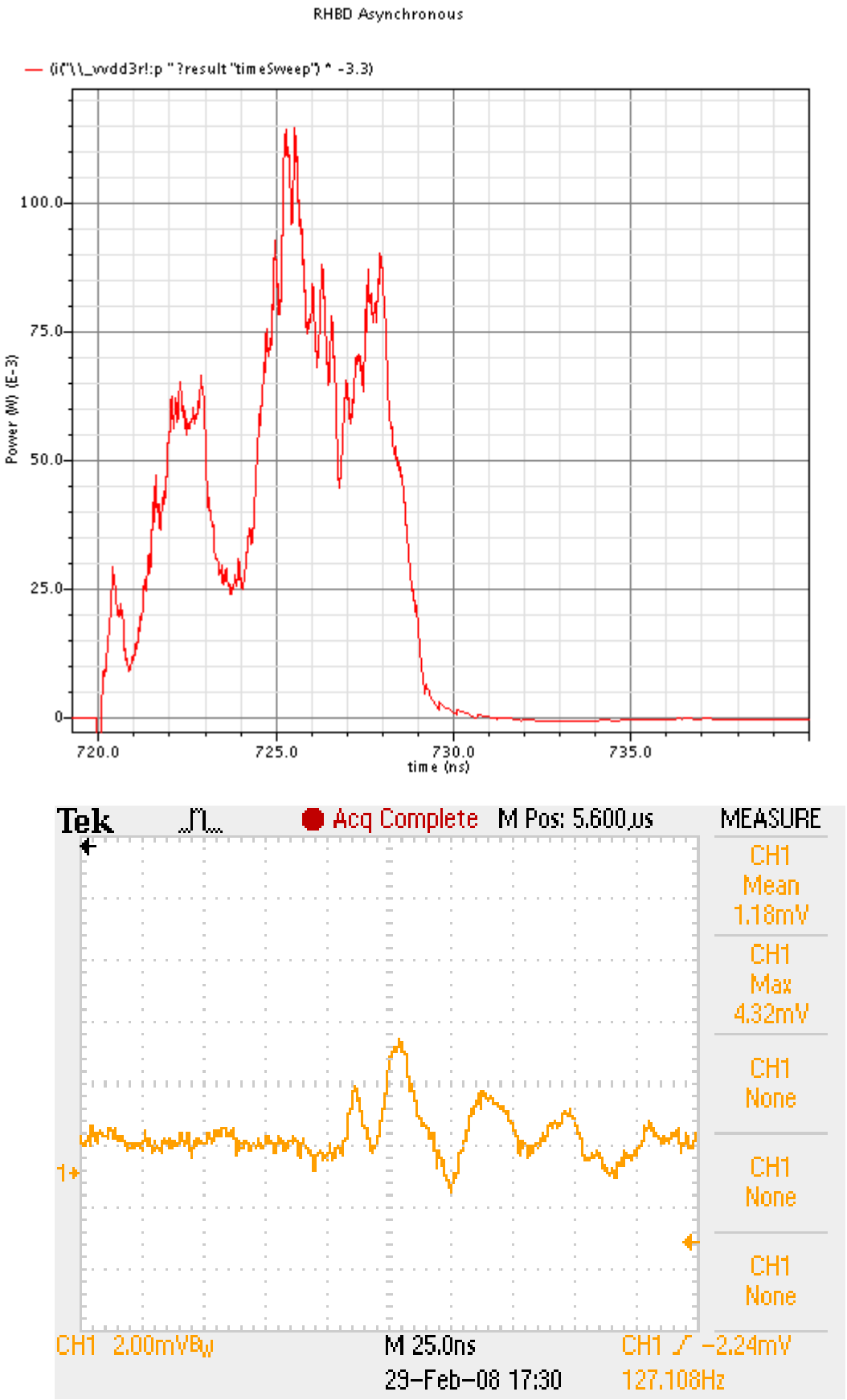


Figure A-27. Test Chip #2AR UltraSim/Hardware Power Comparison (single)

Appendix B. PCBSat Design Data

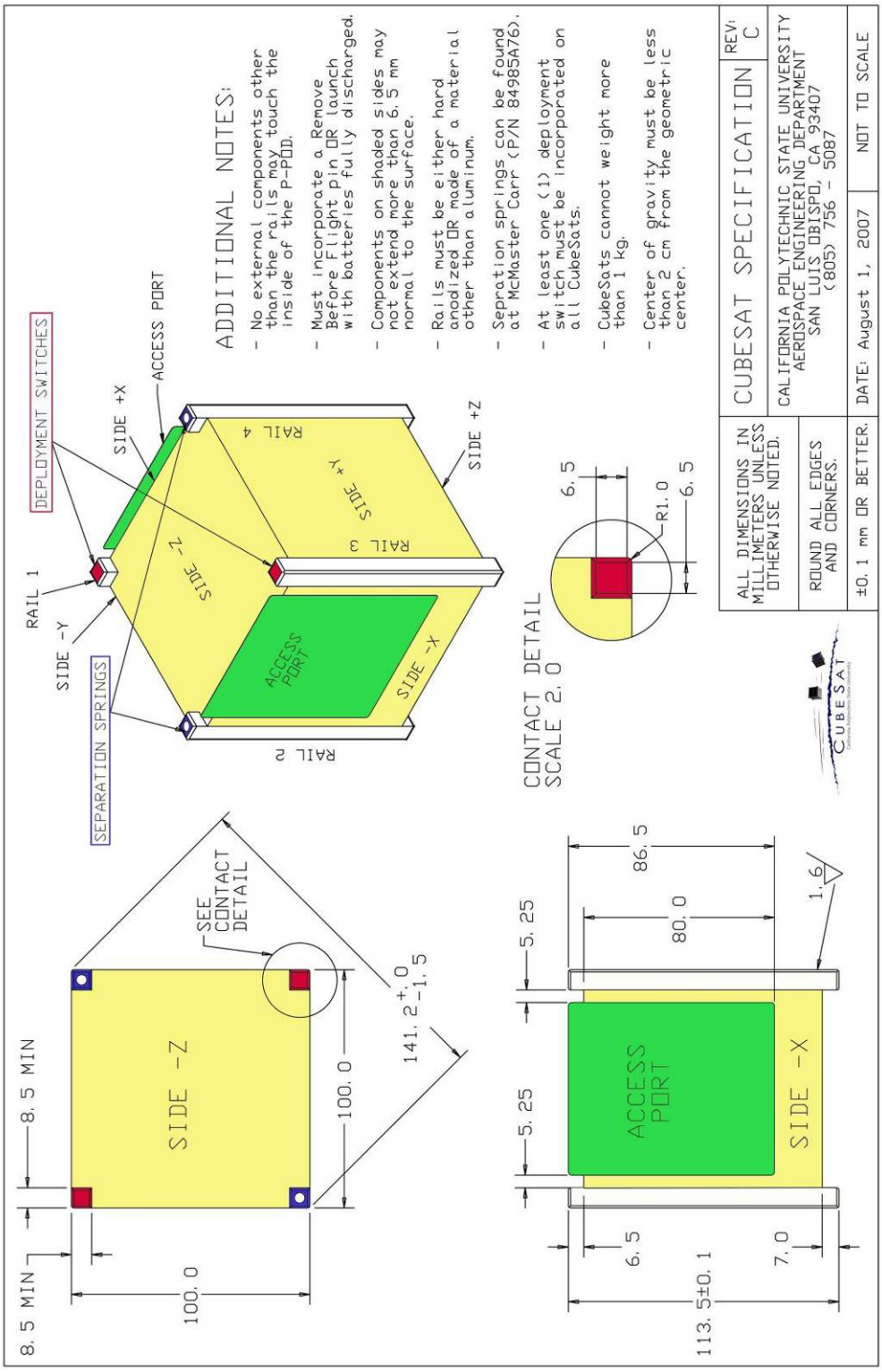


Figure B-1. CubeSat Specification Summary [131]

P/N	Sub	Description	Qty	Mass	Tot Mass	Min Temp	Max Temp	Function	Package	Vendor	Part Number	Qty	1 Ea	1 Ext.	Qty	10 Ea	10 Ext.	Qty	100 Ea	100 Ext.	Qty	1000 Ea	1000 Ext.	Qty	10000 Ea	10000 Ext.
1	EPS	CUSTOM-SPUN 1-LAYER PCB	2	27	54	155	155	Solar Panels	PCB	PrototExpress	n/a	2	$47.50	$95.00	20	$18.50	$37.00	200	$7.00	$14.00	2000	$2.27	$4.54	20000	$1.96	$3.92
1	Payload	CUSTOM-SPUN 1-LAYER PCB	1	0.6	0.6	-55	155	CMOS Imager	PCB	PrototExpress	n/a	1	$0.00	$0.00	10	$0.00	$0.00	100	$0.00	$0.00	1000	$0.00	$0.00	10000	$0.00	$0.00
1	Structure	CUSTOM-SPUN 4-LAYER CORE PCB	1	26	26	-55	155	Core PCB	PCB	PrototExpress	n/a	1	$47.50	$47.50	10	$18.50	$18.50	100	$7.00	$7.00	1000	$2.27	$2.27	10000	$1.96	$1.96
2	DH	RES 0.0 OHM 1/8W 5% 0805 SMD	10	0	0.05	-55	155	GND/AGND link	0805 SMD	Digikey	311-0.0ARCT-ND	10	$0.08	$0.80	100	$0.04	$0.43	1000	$0.02	$0.17	10000	$0.01	$0.05	100000	$0.01	$0.05
3	DH	CAP, 10UF 50V CERAMIC X7R 0805	37	0	0.17	-55	125	Filter caps	0805 SMD	Digikey	311-1140-1-ND	37	$0.10	$3.55	370	$0.06	$2.17	3700	$0.03	$1.02	37000	$0.02	$0.78	370000	$0.02	$0.78
4	EPS	RES 2.20M OHM 1/8W 1% 0805 SMD	6	0	0.03	-55	155	BCR/PPT	0805 SMD	Digikey	311-2.20MCRCT-ND	6	$0.00	$0.00	60	$0.04	$0.26	600	$0.02	$0.15	6000	$0.01	$0.03	60000	$0.01	$0.03
5	EPS	3.6V Panasonic Li-Ion battery	1	13.2	13.2	-20	60	Battery	n/a	Amazon	LI-3ICR/CGA772530	1	$1.99	$1.99	10	$1.99	$1.99	100	$1.99	$1.99	1000	$1.99	$1.99	10000	$1.99	$1.99
6	AOCS	CAP 4.7UF 10V CERAMIC X5R 1206	3	0.01	0.03	-55	125	GPS	1206 SMD	Digikey	PCC226KCT-ND	3	$0.00	$0.00	30	$0.47	$1.42	300	$0.35	$1.04	3000	$0.20	$0.60	30000	$0.20	$0.60
7	DH	RES 10.0K OHM 1/8W 1% 0805 SMD	20	0	0.6	-55	155	Voltage/measure	0805 SMD	Digikey	311-10.0KCRCT-ND	20	$0.03	$0.73	200	$0.01	$0.61	2000	$0.00	$0.49	20000	$0.00	$0.41	200000	$0.00	$0.41
8	AOCS	CAP 1000PF 50V CERAMIC X7R 0805	2	0	0.01	-55	125	GPS ARF	0805 SMD	Digikey	311-1136-1-ND	2	$0.00	$0.00	20	$0.00	$0.00	200	$0.00	$0.00	2000	$0.00	$0.00	20000	$0.00	$0.00
9	AOCS	CAP CER 10UF 10V X5R 1206	2	0.01	0.02	-55	125	in/out filtering for LDO	1206 SMD	Digikey	587-1342-1-ND	2	$0.00	$0.00	20	$0.00	$0.00	200	$0.00	$0.00	2000	$0.00	$0.00	20000	$0.00	$0.00
10	EPS	INDUCTOR 10UH 10% SA TYPE SMD	1	0.02	0.02	-55	125	Creates AVCC	1210 SMD	Digikey	PCD1097CT-ND	1	$0.28	$0.28	10	$0.23	$0.23	100	$0.18	$0.18	1000	$0.12	$0.12	10000	$0.10	$0.10
11	DH	RES 15.0K OHM 1/8W 1% 0805 SMD	4	0	0.02	-55	155	BCR/PPT	0805 SMD	Digikey	311-15.0KCRCT-ND	4	$0.00	$0.00	40	$0.08	$0.32	400	$0.02	$0.10	4000	$0.02	$0.07	40000	$0.01	$0.02
12	EPS	CAP CER 22PF 50V NP0 0805	3	0	0.01	-55	125	CPU clock caps, gps	0805 SMD	Digikey	311-1299-1-ND	3	$0.00	$0.00	30	$0.10	$0.29	300	$0.06	$0.18	3000	$0.03	$0.08	30000	$0.02	$0.06
13	DH	INDUCTOR 22UH 670MA 2220 10%	5	0.4	2	-55	85	BCR/PPT	SMD	Digikey	495-1788-1-ND	5	$0.66	$10.30	50	$1.66	$8.28	500	$1.04	$5.18	5000	$1.04	$5.18	50000	$1.04	$5.18
15	AOCS	RES 24.9K OHM 1/8W 1% 0805 SMD	3	0	0.01	-55	155	Sun sensor	0805 SMD	Digikey	311-24.9KCRCT-ND	3	$0.00	$0.00	30	$0.08	$0.24	300	$0.02	$0.07	3000	$0.02	$0.05	30000	$0.01	$0.02
16	DH	CRYSTAL 32.768 KHZ 6PF SMD	1	0.1	0.1	-40	85	rt clock crystal	SMD	Digikey	300-8341-1-ND	1	$0.66	$0.66	10	$0.57	$0.57	100	$0.38	$0.38	1000	$0.38	$0.38	10000	$0.38	$0.38
17	EPS	RES .05 OHM 1/4W 1% 0805 SMD	4	0	0.02	-55	155	Rsense for ITLM	0805 SMD	Digikey	WSLB-.05CT-ND	4	$1.40	$5.60	40	$1.19	$4.76	400	$0.70	$2.80	4000	$0.56	$2.24	40000	$0.56	$2.24
18	DH	RES 51.0K OHM 1/8W 1% 0805 SMD	2	0	0.01	-55	155	Pullups	0805 SMD	Digikey	311-51.0KCRCT-ND	2	$0.00	$0.00	20	$0.00	$0.00	200	$0.00	$0.00	2000	$0.00	$0.00	20000	$0.00	$0.00
19	EPS	CAP TANT 68UF 16V 10% LOESR SMD	5	0.4	2	-55	125	BCR/PPT	SMD	Digikey	495-1646-1-ND	5	$0.87	$4.35	50	$0.76	$3.81	500	$0.66	$3.32	5000	$0.29	$1.45	50000	$0.29	$1.45
20	EPS	RES 191K OHM 1/8W 1% 0805 SMD	2	0	0.01	-55	155	op amp	0805 SMD	Digikey	311-191KCRCT-ND	2	$0.00	$0.00	20	$0.08	$0.16	200	$0.02	$0.05	2000	$0.03	$0.06	20000	$0.01	$0.01
21	EPS	CAP TANT 220UF 10V 10% LOESR SMD	2	0.4	0.8	-55	125	BCR/PPT	SMD	Digikey	495-1633-1-ND	2	$1.18	$2.36	20	$1.02	$2.05	200	$0.89	$1.79	2000	$0.39	$0.78	20000	$0.39	$0.78
22	EPS	RES 270K OHM 1/8W 1% 0805 SMD	3	0	0.01	-55	155	BCR/PPT	0805 SMD	Digikey	311-270KCRCT-ND	3	$0.00	$0.00	30	$0.05	$0.14	300	$0.03	$0.08	3000	$0.02	$0.07	30000	$0.01	$0.03
23	EPS	LED 1206 ALGAAS RED SMT	1	0	0	-55	155	Red LED	1206 SMD	Digikey	350-1565-1-ND	1	$0.50	$0.50	10	$0.50	$0.50	100	$0.33	$0.33	1000	$0.23	$0.23	10000	$0.23	$0.23
24	DH	IC DATAFLASH 16M 2.7V 8SOIC	1	0.03	0.03	-40	85	flash memory	8SOIC	Digikey	AT45DB161D-SU-ND	1	$2.52	$2.52	10	$2.52	$2.52	100	$1.66	$1.66	1000	$1.66	$1.66	10000	$1.66	$1.66
25	Payload	XS6502D15T2 CMOS imager	1	0.6	0.6	0	40	CMOS Imager	14SMOP	Digikey	obsolete	1	$21.00	$21.00	10	$21.00	$21.00	100	$21.00	$21.00	1000	$21.00	$21.00	10000	$21.00	$21.00
26	Payload	XSD15T8 CMOS imager socket	1	0.2	0.2	0	40	socket	14SMOP	Digikey	obsolete	1	$1.43	$1.43	10	$1.43	$1.43	100	$1.43	$1.43	1000	$1.43	$1.43	10000	$1.43	$1.43
27	Payload	CONN HEADER 2MM DUAL R/A 14POS	1	0.4	0.4	-40	105	camera interface	thru hole	Digikey	S5803-07-ND	1	$1.54	$1.54	10	$1.33	$1.33	100	$1.13	$1.13	1000	$0.73	$0.73	10000	$0.73	$0.73
28	DH	IC TIMEKEEPER T-CHARGE IND 8SOIC	1	0.03	0.03	-40	85	rt clock	8SOIC	Digikey	DS1302ZN+-ND	1	$2.66	$2.66	10	$2.66	$2.66	100	$2.11	$2.11	1000	$2.11	$2.11	10000	$2.11	$2.11
29	AOCS	Fastrax GPS Module	1	1.6	1.6	-40	85	GPS Module	SMT	Fastrax	ITRAX03-S	1	$40.00	$40.00	10	$36.40	$36.40	100	$36.40	$36.40	1000	$36.40	$36.40	10000	$36.40	$36.40
30	DH	LED 1206 ALGAAS RED SMT	1	0	0	-55	155	Red LED	1206 SMD	Digikey	350-1565-1-ND	1	$0.50	$0.50	10	$0.50	$0.50	100	$0.33	$0.33	1000	$0.23	$0.23	10000	$0.23	$0.23
31	AOCS	IC REG ULTRA LDO 150MA SOT-23-5	1	0.02	0.02	-40	125	GPS ARF	SOT-23-5	Digikey	LP3985IM5-2.8CT-ND	1	$1.04	$1.04	10	$1.04	$1.04	100	$0.54	$0.54	1000	$0.32	$0.32	10000	$0.32	$0.32
32	EPS	IC LDO REG LOW-IQ 3.3V/ADJ 8SOIC	1	0.03	0.03	-40	85	3.3V voltage regulator	8SOIC	Digikey	MAX604CSA+ND	1	$4.77	$4.77	10	$4.77	$4.77	100	$2.12	$2.12	1000	$2.12	$2.12	10000	$2.19	$2.19
33	EPS	IC DC/DC CONV STPUP 3.365V 8SOIC	2	0.03	0.07	-40	85	BCR/PPT	8SOIC	Digikey	MAX856CSA+ND	2	$4.13	$8.26	20	$4.13	$8.26	200	$1.83	$3.66	2000	$1.83	$3.66	20000	$1.91	$3.81
34	EPS	IC P-CHANNEL SWITCH 8-UMAX	1	0.03	0.03	-40	85	sw/sel shdn/reset	MSOP8	Digikey	MAX892LEUA+ND	1	$3.62	$3.62	10	$3.62	$3.62	100	$1.92	$1.92	1000	$1.92	$1.92	10000	$1.92	$1.92
35	EPS	IC COMPARATOR 0/0 8-SOIC	2	0.03	0.07	-40	85	BCR/PPT	8SOIC	MaxDirect	MAX962CSA+ND	2	$1.40	$2.80	20	$1.40	$2.80	200	$1.40	$2.80	2000	$1.40	$2.80	20000	$1.47	$2.95
36	EPS	Bidirectional, High-Side, Current-S	4	0.03	0.13	-40	85	telemetry	MSOP8	MaxDirect	MAX4072AUA+	4	$1.52	$6.08	40	$1.33	$5.32	400	$0.94	$3.76	4000	$0.85	$3.40	40000	$0.85	$3.40
37	EPS	IC MUX ANLG CMOS 4OHM 4CH 16UMAX	2	0.03	0.07	-40	85	telemetry	16umax	Digikey	MAX4634EUE+ND	2	$3.06	$6.12	20	$3.06	$6.12	200	$1.36	$2.71	2000	$1.36	$2.71	20000	$1.36	$2.71
38	MESA	CONN HEADER 120PIN 2MM SMD LOCK	1	0.6	0.6	-55	125	Mega128L	TQFP64	Digikey	A26613-64-128-8AU-ND	1	$15.95	$15.95	10	$15.95	$15.95	100	$9.75	$9.75	1000	$9.75	$9.75	10000	$9.75	$9.75
39	MESA	CONN RECEPT 2MM SINGLE R/A 14POS	2	0.1	0.2	-40	105	mesa interface	thru hole	Digikey	S5602-14-ND	2	$1.60	$3.20	20	$1.46	$2.92	200	$0.86	$1.73	2000	$0.49	$0.98	20000	$0.49	$0.98
40	MESA	CONN RECEPT 2MM SINGLE SMD 5POS	2	0.1	0.2	-40	105	mesa interface	SMD	Digikey	S5602-05-ND	2	$1.60	$3.20	20	$1.36	$2.71	200	$0.86	$1.73	2000	$1.24	$2.48	20000	$0.62	$1.24
41	EPS	POLYSWITCH 0.75A RESET FUSE SMD	1	0.01	0.01	-55	125	poly/switch	1206 SMD	Digikey	NANOSMDC075F-CT-ND	1	$0.50	$0.50	10	$0.44	$0.44	100	$0.40	$0.40	1000	$0.33	$0.33	10000	$0.33	$0.33
42	EPS	SWITCH DETECT PB SPST-NO RT ANG	1	0.05	0.05	-20	60	RBF switch	SMT	Digikey	401-1738-ND	1	$2.10	$2.10	10	$1.33	$1.33	100	$0.91	$0.91	1000	$0.91	$0.91	10000	$0.91	$0.91
43	EPS	CONN RECEPT 2MM SINGLE SMD 7POS	2	0.1	0.2	-40	105	solar panel interface	SMT	Digikey	S5902-07-ND	2	$1.64	$3.28	20	$1.36	$2.71	200	$0.86	$1.73	2000	$0.62	$1.24	20000	$0.62	$1.24
44	EPS	CONN HEADER 2MM SINGLE STR 7POS	2	0.1	0.2	-40	105	solar panel interface	thru hole	Digikey	S5800-07-ND	2	$0.52	$1.04	20	$0.45	$0.90	200	$0.38	$0.76	2000	$0.25	$0.49	20000	$0.25	$0.49
45	AOCS	GEOHELIX-SMP PASS GPS ANT	1	9.4	9.4	-40	85	GPS Antenna	SMT	3D01	1010004	1	$10.40	$10.40	10	$10.40	$10.40	100	$10.40	$10.40	1000	$10.40	$10.40	10000	$10.40	$10.40
46	DH	BATTERY LITH 3V RECHARGE W/LEGS	1	0.08	0.08	-20	60	Clock battery	SMT	Digikey	P0MCT-ND	1	$2.55	$2.55	10	$2.13	$2.13	100	$1.70	$1.70	1000	$1.28	$1.28	10000	$1.28	$1.28
47	TCS	THERMISTOR NTC 10K OHM 5% TOLER	6	0.01	0.03	-80	150	SP, Batt	axial	Digikey	235-1002-ND	6	$4.29	$25.74	60	$3.38	$20.26	600	$1.45	$8.68	6000	$1.34	$8.04	60000	$1.34	$8.04
48	GSE	CONN HEADER 2MM SINGLE R/A 12POS	1	0.4	0.4	-40	105	gse	thru hole	Digikey	S5802-12-ND	1	$0.50	$0.50	10	$0.44	$0.44	100	$0.49	$0.49	1000	$0.24	$0.24	10000	$0.22	$0.22
49	GSE	CONN RECEPT 2MM SINGLE R/A 12POS	1	na	na	na	na	gse	smt	Digikey	S5752-12-ND	1	$2.20	$2.20	10	$1.83	$1.83	100	$1.16	$1.16	1000	$0.84	$0.84	10000	$0.84	$0.84
50	Comm	CONN RECEPT 2MM DUAL SMD 12POS	1	0.4	0.4	-40	105	xtend interface	smt	Digikey	S6013-10-ND	1	$3.38	$3.38	10	$2.80	$2.80	100	$1.78	$1.78	1000	$1.28	$1.28	10000	$1.28	$1.28
51	GSE	CONN HEADER 6POS .100" VERT 15AU	3	na	na	na	na	Programming Jumpers	SMT	Digikey	WM17457-ND	3	$0.77	$2.31	30	$0.68	$2.04	300	$0.45	$1.36	3000	$0.30	$0.90	30000	$0.27	$0.82
52	GSE	HEADER, R/A 6WAY (Hirting)	1	na	na	na	na	ISP port	0.1" TH	Farnell iniOne	1094979	1	$0.38	$0.38	10	$0.33	$0.33	100	$0.25	$0.25	1000	$0.19	$0.19	10000	$0.17	$0.17
53	GSE	CONN JACK POWER 2.1MM PCB	1	na	na	na	na	VCC	SMT	CP-102A-ND	CP-102A-ND	1	$1.00	$1.00	10	$0.85	$0.85	100	$0.65	$0.65	1000	$0.49	$0.49	10000	$0.49	$0.49
54	AOCS	SWITCH TACTILE SPST-NO 0.05A 4CT SM	1	0.05	0.05	-40	125	Sep switch	SMT	PV-9908-ND	PV-9908-ND	1	$1.70	$1.70	10	$1.70	$1.70	100	$1.70	$1.70	1000	$1.28	$1.28	10000	$1.28	$1.28
55	AOCS	PHOTOCELL 10K-200K OHM 4.2MM	2	0	0	-30	75	Sun sensor	axial	Digikey	PDV-P9008-ND	2	$1.77	$3.54	20	$1.77	$3.54	200	$1.77	$3.54	2000	$1.77	$3.54	20000	$0.89	$1.67
56	GSE	CONN HEADER 4POS .100" R/A GOLD	1	na	na	na	na	UMB port	0.1" TH	Digikey	WM6110-ND	1	$0.71	$0.71	10	$0.63	$0.63	100	$0.42	$0.42	1000	$0.28	$0.28	10000	$0.25	$0.25
59	GSE	Brainstem	1	na	na	na	na	UMB port																		
														Subsystem PCB Total:		$242.61	**$355.31**		$177.76	**$252.33**		$136.13	**$177.58**		$112.63	**$140.94**		$112.05	**$139.99**
														Less PCB			$290.31			$215.33			$163.58			$136.40			$136.07
59	MESA	CAP CER 1UF 50V X7R 10% 1206	2	0.01	0.02	-55	125	Filter caps	1206 SMD	Digikey	445-1423-1-ND	2	$0.00	$0.00	20	$0.44	$0.87	200	$0.26	$0.52	2000	$0.07	$0.14	20000	$0.07	$0.14
60	MESA	DIODE ZENER 350MW 3.0V SOT23	2	0.02	0.03	-65	150	3v zener diode	SOT23	Digikey	MMBZ5225B-FDICT-ND	2	$1.30	$2.60	20	$1.13	$2.25	200	$0.98	$1.97	2000	$0.42	$0.83	20000	$0.40	$0.80
61	MESA	CAP TANT 4.7UF 50V 10% LOESR SMD	1	0.4	0.4	-55	125	+36V power supply	SMD	Digikey	495-1586-1-ND	1	$0.00	$0.00	10	$0.39	$0.39	100	$0.23	$0.23	1000	$0.13	$0.13	10000	$0.06	$0.06
62	MESA	RES 36.5K OHM 1/8W 1% 0805 SMD	2	0	0.01	-55	155	op amp	0805 SMD	Digikey	311-36.5KCRCT-ND	2	$0.00	$0.00	20	$0.08	$0.16	200	$0.02	$0.05	2000	$0.03	$0.06	20000	$0.01	$0.01
63	MESA	RES 42.2K OHM 1/8W 1% 0805 SMD	2	0	0.01	-55	155	op amp	0805 SMD	Digikey	311-42.2KCRCT-ND	2	$0.00	$0.00	20	$0.08	$0.16	200	$0.02	$0.05	2000	$0.03	$0.06	20000	$0.01	$0.01
64	MESA	RES 90.9K OHM 1/8W 1% 0805 SMD	1	0	0	-55	155	op amp	0805 SMD	Digikey	311-90.9KCRCT-ND	1	$0.00	$0.00	10	$0.08	$0.08	100	$0.04	$0.04	1000	$0.02	$0.02	10000	$0.01	$0.01
65	MESA	RES 100K OHM 1/8W 1% 0805 SMD	15	0	0.07	-55	155	op amp	0805 SMD	Digikey	311-100KCRCT-ND	15	$0.00	$0.00	150	$0.04	$0.65	1500	$0.02	$0.25	15000	$0.01	$0.08	150000	$0.01	$0.08
66	MESA	RES 2.20K OHM 1/4W 1% 0805 SMD	1	0	0	-55	155	+36V power supply	0805 SMD	Digikey	RL1225-122FC-ND	1	$1.40	$1.40	10	$1.19	$1.19	100	$0.92	$0.92	1000	$0.56	$0.56	10000	$0.56	$0.56
67	MESA	CAP TANT 150UF 16V 10% LOESR SMD	1	0.4	0.4	-55	125	+36V power supply	SMD	Digikey	495-1592-1-ND	1	$0.00	$0.00	10	$0.00	$0.00	100	$0.00	$0.00	1000	$0.00	$0.00	10000	$0.00	$0.00
68	MESA	RES 220K OHM 1/8W 1% 0805 SMD	4	0	0.02	-55	155	op amp	0805 SMD	Digikey	311-220KCRCT-ND	4	$0.00	$0.00	40	$0.08	$0.32	400	$0.02	$0.10	4000	$0.02	$0.07	40000	$0.01	$0.02
69	MESA	RES 402K OHM 1/8W 1% 0805 SMD	3	0	0.01	-55	155	BCR/PPT	0805 SMD	Digikey	311-402KCRCT-ND	3	$0.00	$0.00	30	$0.05	$0.14	300	$0.03	$0.08	3000	$0.02	$0.07	30000	$0.01	$0.03
70	MESA	IC LOW PWR FET INST AMP 8-SOIC	1	0.03	0.03	-40	85	op amp	8SOIC	Digikey	INA121U-ND	1	$7.52	$15.04	20	$7.52	$15.04	200	$5.08	$10.16	2000	$4.78	$9.56	20000	$4.78	$9.56
71	MESA	IC D/A CONV 12BIT R-R DUAL 8SOIC	1	0.03	0.03	-40	85	d/a	8SOIC	Linear	LTC1664I	1	$13.63	$13.63	10	$13.63	$13.63	100	$7.45	$7.45	1000	$7.45	$7.45	10000	$7.50	$7.50
72	MESA	IC PWM CTRLR STEP-UP 1.8V 10UMAX	1	0.03	0.03	-40	85	+36V power supply	10umax	Digikey	MAX668EUB+ND	1	$5.76	$5.76	10	$5.76	$5.76	100	$2.61	$2.61	1000	$2.61	$2.61	10000	$2.61	$2.61
73	MESA	IC DC/DC CONV STEP-UP 12V 8-SOIC	1	0.03	0.03	-40	85	+12V power supply	8SOIC	Digikey	MAX761ESA+ND	1	$8.62	$8.62	10	$8.62	$8.62	100	$3.91	$3.91	1000	$3.91	$3.91	10000	$3.91	$3.91
74	MESA	IC DC/DC INV -12V HI-EFF 8-SOIC	1	0.03	0.03	-40	85	-12V power supply	8SOIC	Digikey	MAX765ESA+ND	1	$9.32	$9.32	10	$9.32	$9.32	100	$4.14	$4.14	1000	$4.14	$4.14	10000	$4.14	$4.14
75	MESA	IC LDO V-REF PREC MCRPWR 8-SOIC	1	0.03	0.03	-40	85	prec. Voltage ref	8SOIC	Digikey	MAX6192AESA+ND	1	$6.66	$6.66	10	$6.66	$6.66	100	$2.95	$2.95	1000	$2.95	$2.95	10000	$2.95	$2.95
76	MESA	IC A/D SRL 4CH 12BIT 2.7V 16QSOP	1	0.05	0.05	-40	85	a/d	16QSOP	Digikey	MAX1247BCEE+ND	1	$15.90	$15.90	10	$15.90	$15.90	100	$7.69	$7.69	1000	$7.69	$7.69	10000	$7.69	$7.69
77	MESA	IRLML2502PBF,CT-ND	1	0.02	0.02	-55	150	+36V power supply	SMD	Digikey	IRLML2502PBFCT-ND	1	$0.82	$0.82	10	$0.48	$0.48	100	$0.32	$0.32	1000	$0.21	$0.21	10000	$0.21	$0.21
78	MESA	IC SINGLE SUPPLY OPAMP 8-SOIC	5	0.03	0.17	-40	85	op amp	8SOIC	Digikey	OPA2340UA-ND	5	$3.22	$16.10	50	$3.22	$16.10	500	$1.80	$8.01	5000	$1.80	$8.01	50000	$1.80	$8.01
80	MESA	DIODE SCHOTTKY 40V 1.0A SOT-23	7	0.02	0.11	-55	125	all power supplies	SMD	Digikey	ZHCS1000CT-ND	7	$1.04	$7.28	70	$0.78	$5.46	700	$0.37	$2.56	7000	$0.30	$2.07	70000	$0.30	$2.07
														Payload PCB Total:		$74.64	**$102.60**		$74.27	**$100.39**		$39.51	**$60.05**		$35.78	**$50.72**		$36.77	**$50.64**

Figure B-2. PCBSat Detailed Parts List

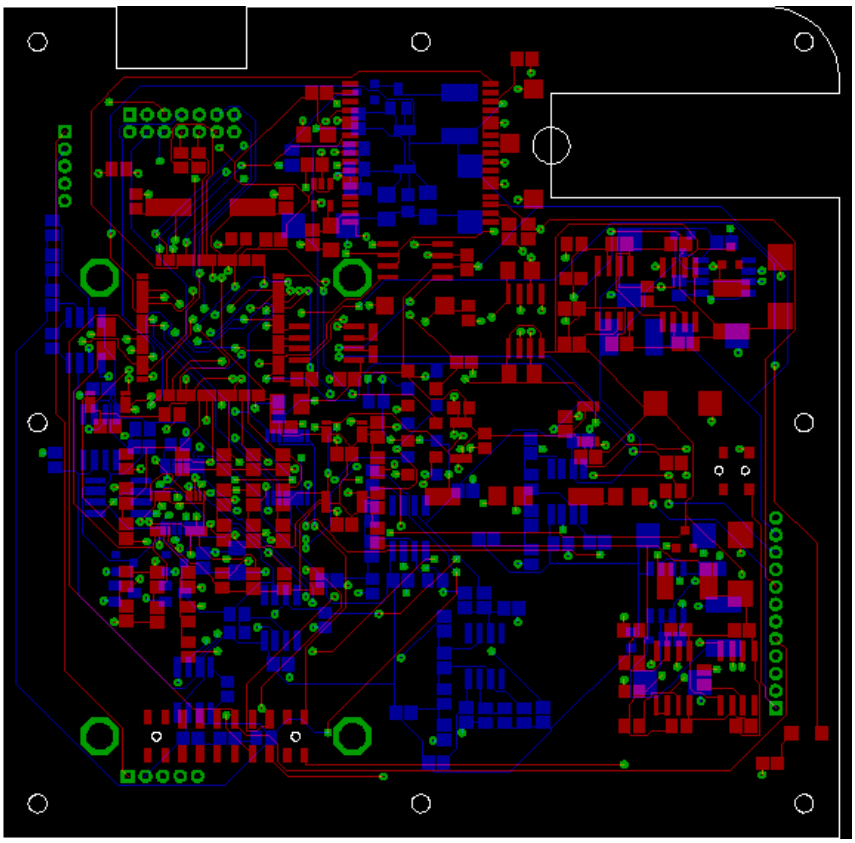


Figure B-3. PCBSat Core PCB Top and Bottom Layers

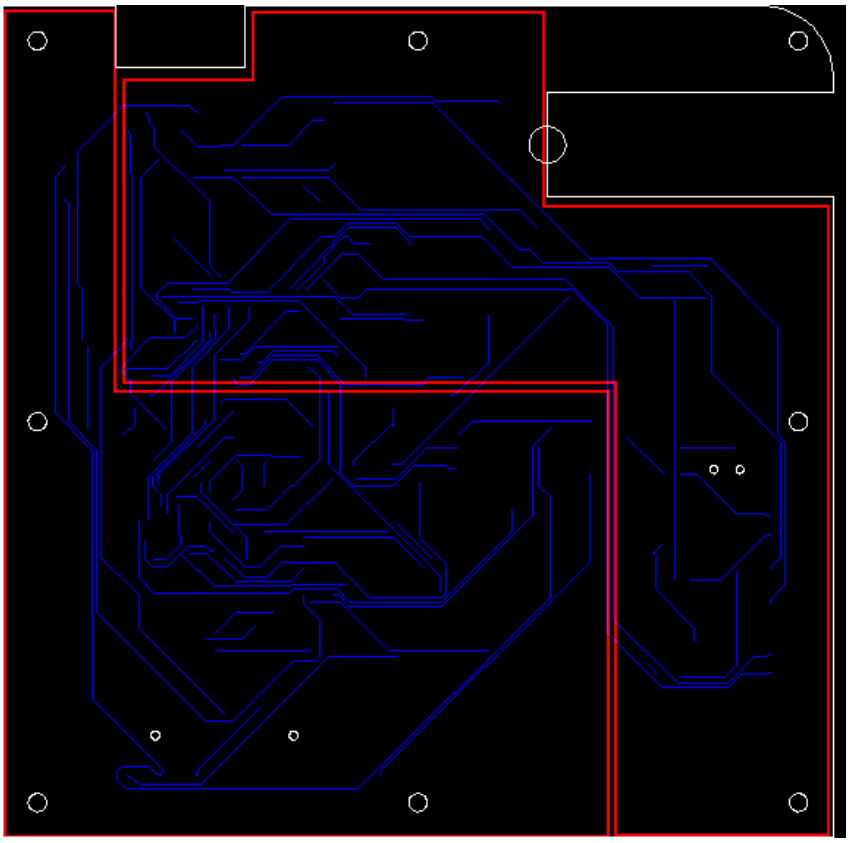


Figure B-4. PCBSat Core PCB Ground and Inner Signal Layers

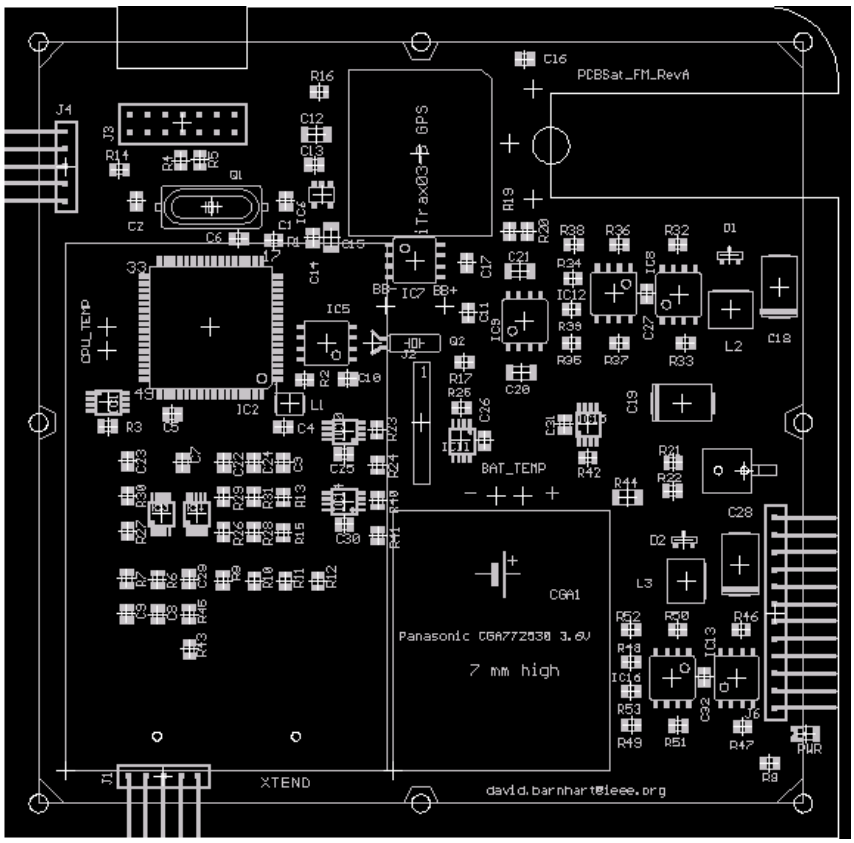


Figure B-5. PCBSat Core PCB Top Part Placement

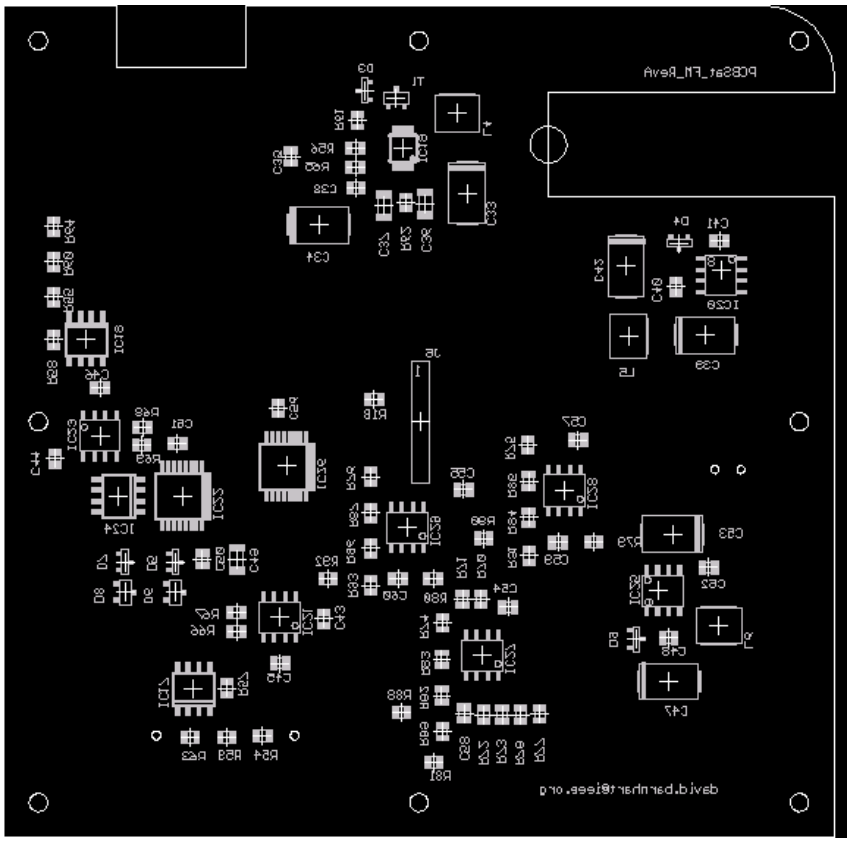


Figure B-6. PCBSat Core PCB Bottom Part Placement

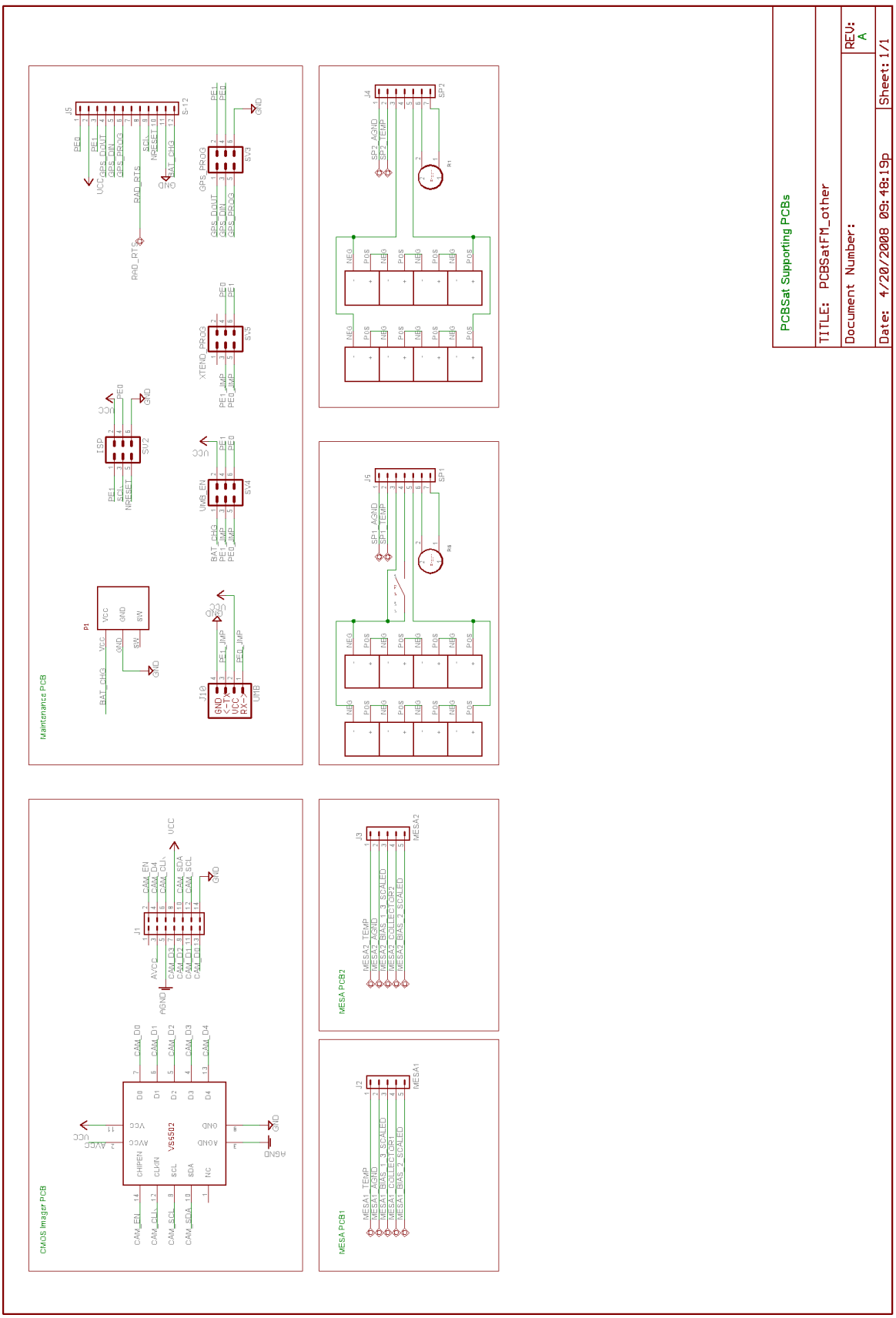


Figure B-7. PCBSat Supporting PCBs Schematic

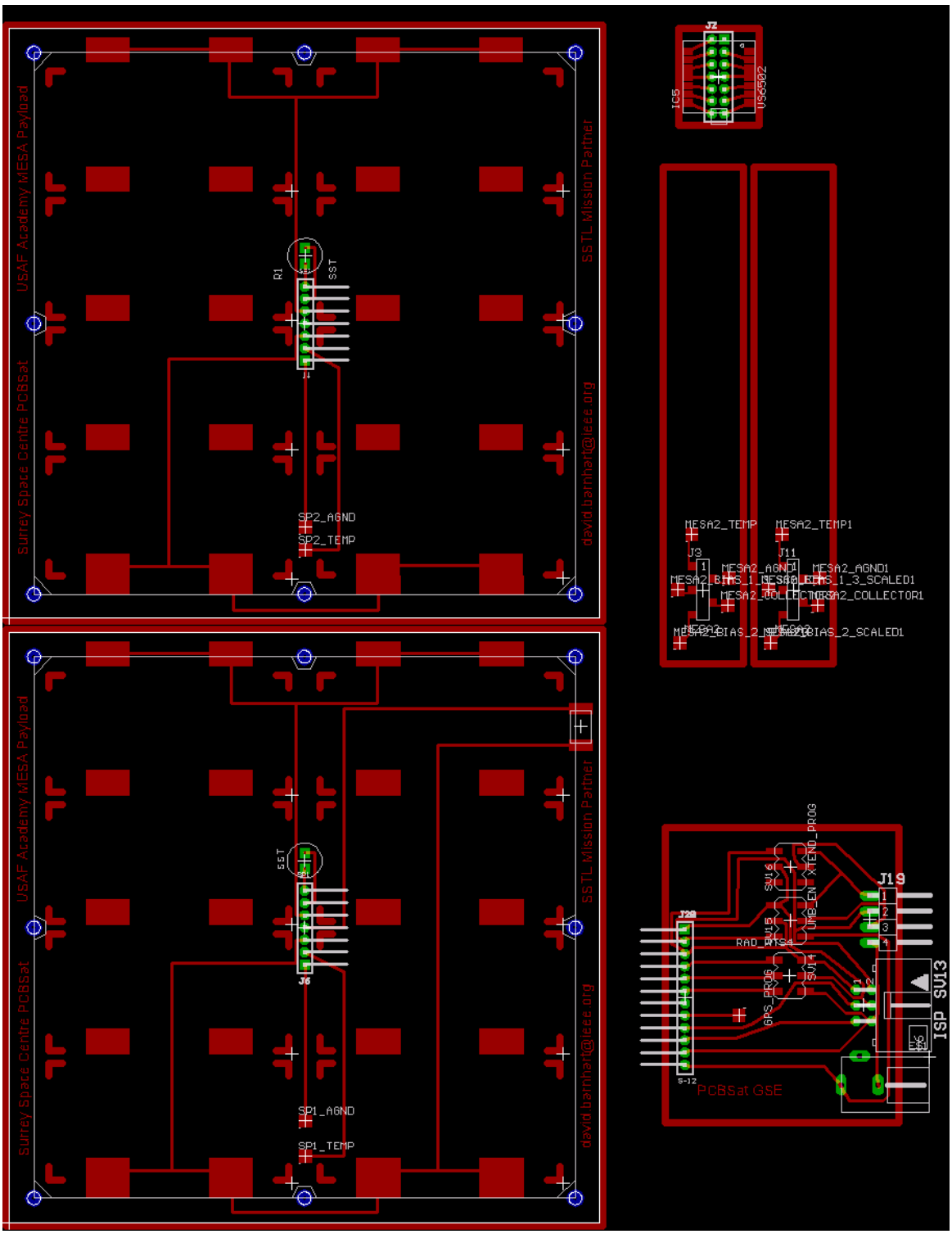
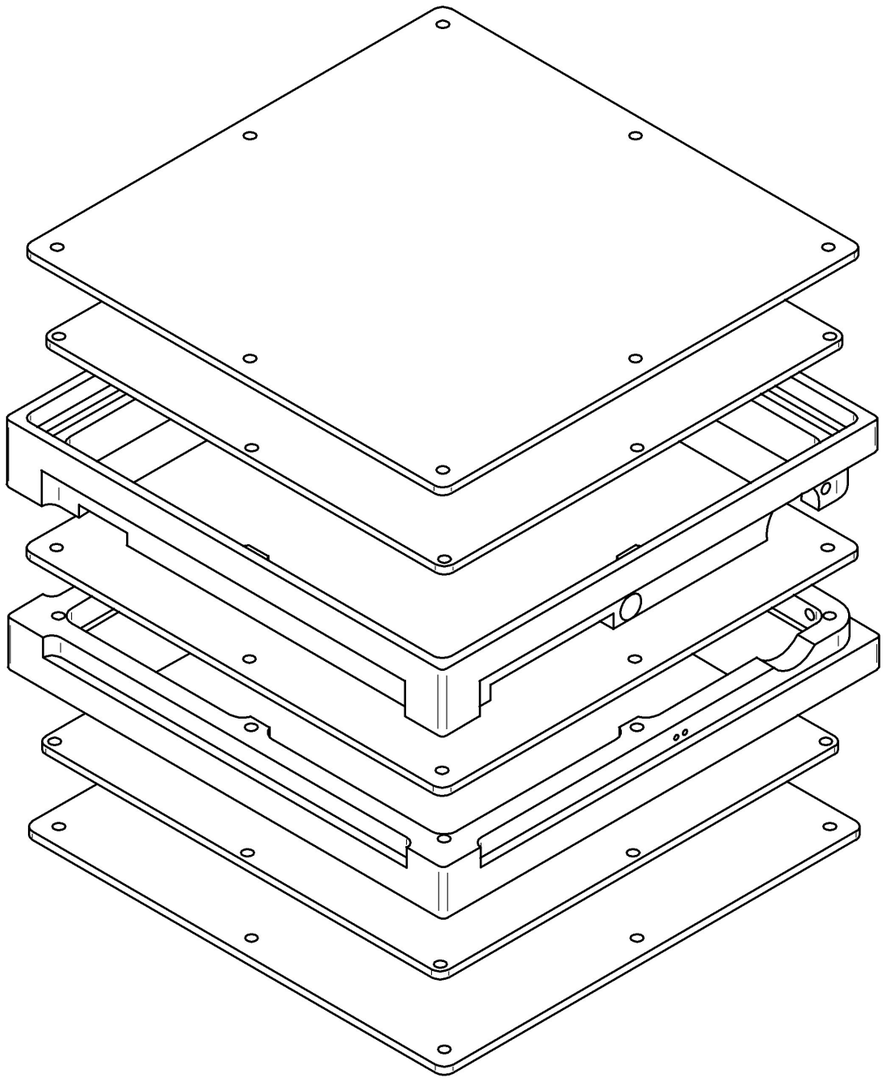
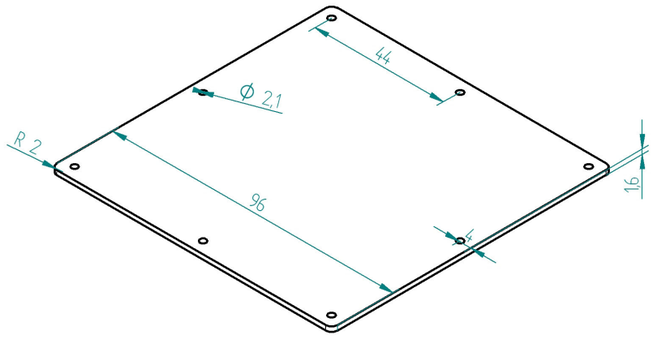


Figure B-8. PCBSat Supporting PCBs Layout

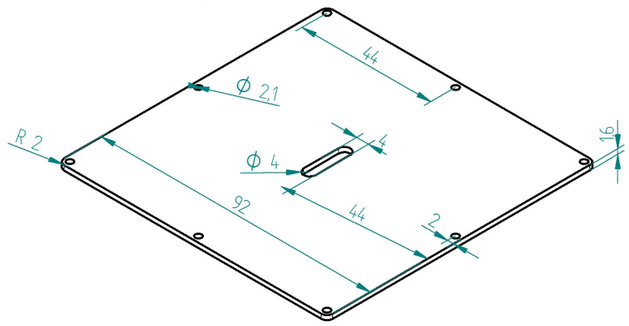
REVISION HISTORY			
REV	DESCRIPTION	DATE	APPROVED



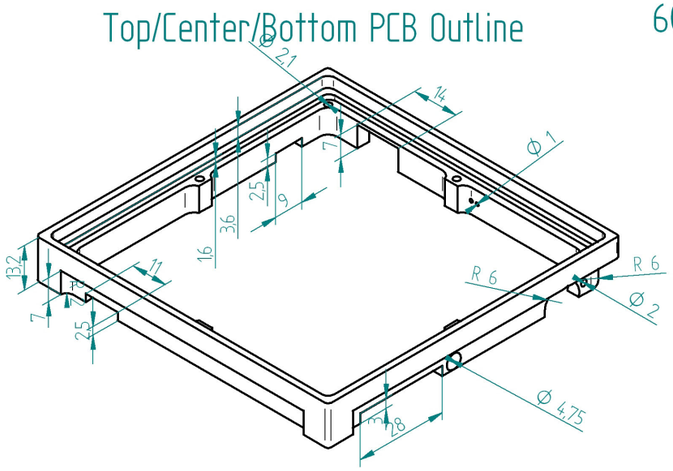
PCBSat Assembly



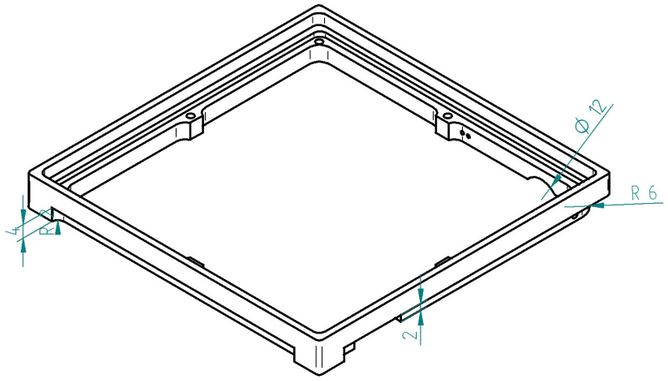
Top/Center/Bottom PCB Outline



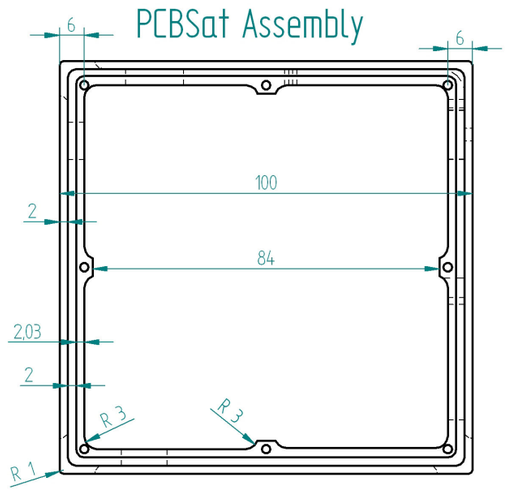
6061 or 6082 Aluminum for Thermal/Radiation/RF



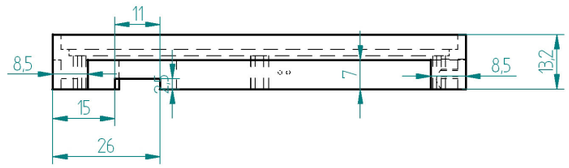
Delrin Top Spacer

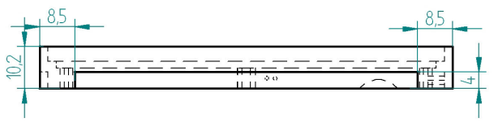


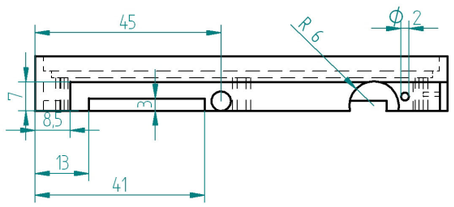
Delrin Bottom Spacer

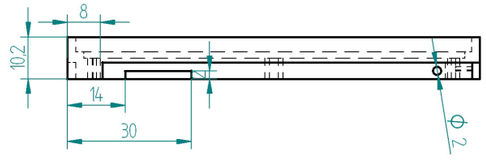


Delrin Spacer Common Dimensions









	NAME	DATE
DRAWN	pc106	06/24/08
CHECKED		
ENG APPR		
MGR APPR		

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN MILLIMETERS
ANGLES ±X.X°
2 PL ±X.XX 3 PL ±X.XXX

SOLID EDGE
UGS - The PLM Company

TITLE

SIZE	DWG NO	REV
A2		

FILE NAME: PCBSat Assembly.dft

SCALE:	WEIGHT:	SHEET 1 OF 1